EXHIBIT H

Exhibit A-26
Invalidity Claim Chart for U.S. Patent No. 7,924,802 vs. U.S. Patent Application Publication No. 2010/0062726

U.S. Patent Application Publication No. 2010/0062726 ("Zheng") was filed on November 22, 2006 and published no later than March 11, 2010. Zheng anticipates asserted claims 1–4, 6–10, 13, 14, 17, and 21–24 of U.S. Patent No. 7,924,802 ("the '802 Patent") under 35 U.S.C. § 102. Zheng also renders obvious asserted claims 1–4, 6–10, 13, 14, 17, and 21–24 of the '802 Patent under 35 U.S.C. § 103, alone based on the state of the art and/or in combination with one or more other references identified in Exs. A-1–A-31, Cover Pleading, and First Supplemental Ex. A-Obviousness Chart.[1]

To the extent Plaintiff alleges that Zheng does not disclose any particular limitation of the asserted claims in the '802 Patent, either expressly or inherently, it would have been obvious to a person of ordinary skill in the art as of the priority date of the '802 Patent to modify Zheng and/or to combine the teachings of Zheng with other prior art references, including but not limited to the present prior art references found in Exs. A-1–A-31, Cover Pleading, First Supplemental Ex. A-Obviousness Chart, and the relevant section of charts for other prior art for the '802 Patent in a manner that would render the asserted claims of these patents invalid as obvious.

With respect to the obviousness of the asserted claims of the '802 Patent under 35 U.S.C. § 103, one or more of the principles enumerated by the United States Supreme Court in *KSR v. Teleflex*, 550 U.S. 398 (2007) apply, including: (a) combining various claimed elements known in the prior art according to known methods to yield a predictable result; and/or (b) making a simple substitution of one or more known elements for another to obtain a predictable result; and/or (c) using a known technique to improve a similar device or method in the same way; and/or (d) applying a known technique to a known device or method ready for improvement to yield a predictable result; and/or (e) choosing from a finite number of identified, predictable solutions with a reasonable expectation of success or, in other words, the solution was one which was "obvious to try"; and/or (f) a known work in one field of endeavor prompting variations of it for use either in the same field or a different field based on given design incentives or other market forces in which the variations were predictable to one of ordinary skill in the art; and/or (g) a teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill in the art to modify the prior art reference or to combine the teachings of various prior art references to arrive at the claimed invention. It therefore would have been obvious to one of ordinary skill in the art to combine the disclosures of these references in accordance with the principles and rationales set forth above.

[1] Samsung is investigating this prior art and has not yet completed discovery from third parties, who may have relevant information concerning the prior art, and therefore, Samsung reserves the right to supplement this chart after additional discovery is received. To the extent that any of the prior art discloses the same or similar functionality or feature(s) of any of the accused products, Samsung reserves the right to argue that said feature or functionality does not practice any limitation of any of the asserted claims, and to argue, in the alternative, that if said feature or functionality is found to practice any limitation of any of the asserted claims in the '802 Patent, then the prior art reference teaches the limitation and that the claim is not patentable.

The citations to portions of any reference in this chart are exemplary only. For example, a citation that refers to or discusses a figure or figure item should be understood to also incorporate by reference that figure and any additional descriptions of that figure as if set forth fully therein. Samsung reserves the right to rely on the entirety of the references cited in this chart to show that the asserted claims of the '802 Patent are invalid. Citations presented for one claim limitation are expressly incorporated by reference into all other limitations for that claim as well as all limitations of all claims on which that claim depends. Samsung also reserves the right to rely on additional citations or sources of evidence that also may be applicable, or that may become applicable in light of claim construction, changes in Plaintiff's infringement contentions, and/or information obtained during discovery as the case progresses.

Claim 1 of the '802 Patent	**Prior Art Reference – Zheng**
[1.1] A method of transmitting information in a wireless communication channel comprising:	To the extent the preamble is limiting, Zheng discloses "A method of transmitting information in a wireless communication channel comprising." See, e.g.: In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137.

Claim 1 of the '802 Patent	Prior Art Reference – Zheng
	The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.
[1.2] transmitting first information across a first frequency range using a wireless transmitter, the first frequency range having a first center frequency, a first highest frequency, and a first lowest frequency; and	Zheng discloses "transmitting first information across a first frequency range using a wireless transmitter, the first frequency range having a first center frequency, a first highest frequency, and a first lowest frequency." See, e.g.:

Claim 1 of the '802 Patent	Prior Art Reference – Zheng

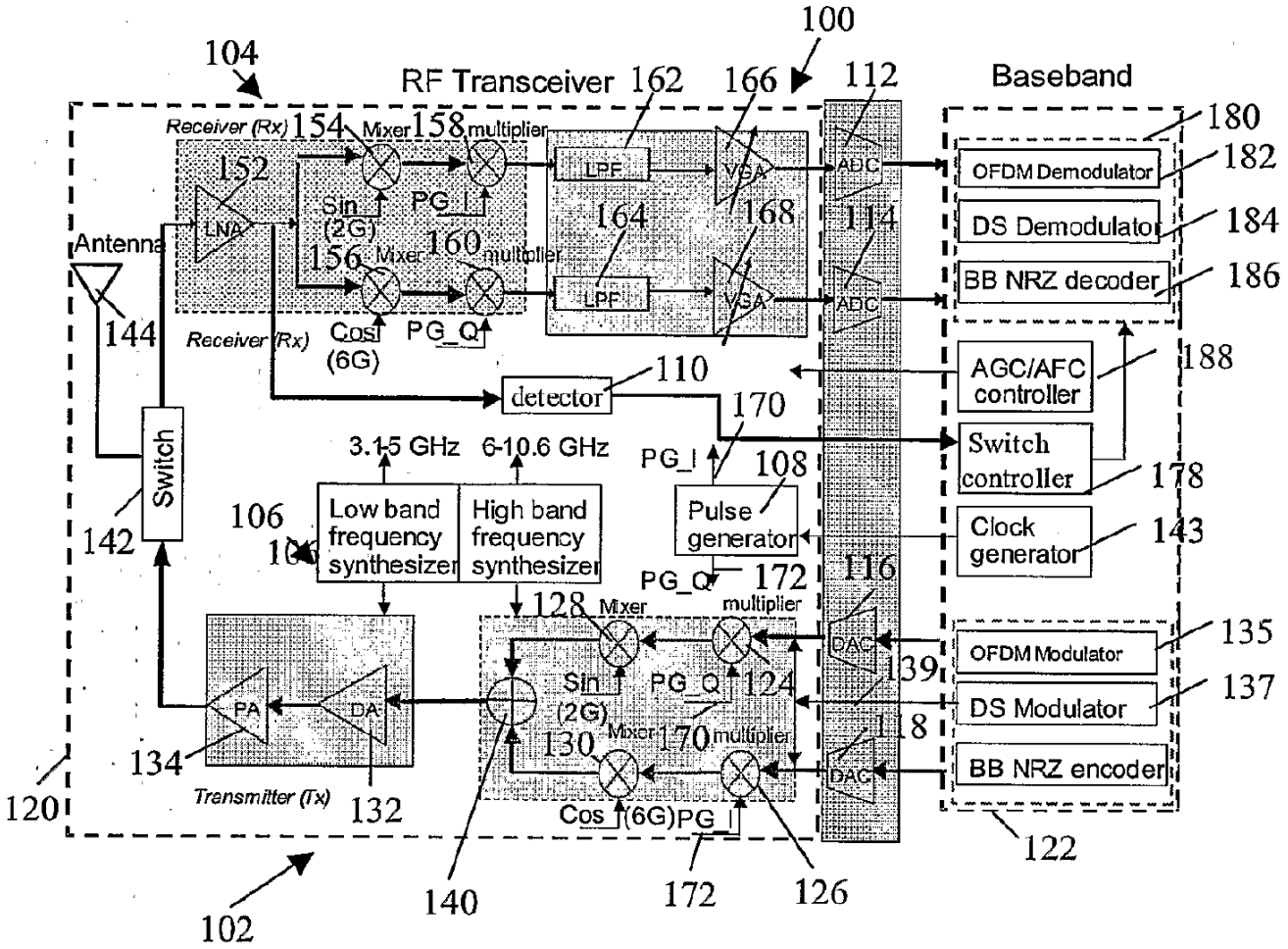


Figure 1

See, e.g., Zheng at Figure 1.

Claim 1 of the '802 Patent	Prior Art Reference – Zheng
	In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027].

Claim 1 of the '802 Patent	Prior Art Reference – Zheng
	The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5)

Claim 1 of the '802 Patent	Prior Art Reference – Zheng
	where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.
[1.3] simultaneously transmitting second information across a second frequency range using the same wireless transmitter, the second frequency range having a second center frequency greater than the first center frequency, a second highest frequency, and a second lowest frequency.	Zheng discloses "simultaneously transmitting second information across a second frequency range using the same wireless transmitter, the second frequency range having a second center frequency greater than the first center frequency, a second highest frequency, and a second lowest frequency." See, e.g.:

Claim 1 of the '802 Patent	Prior Art Reference – Zheng

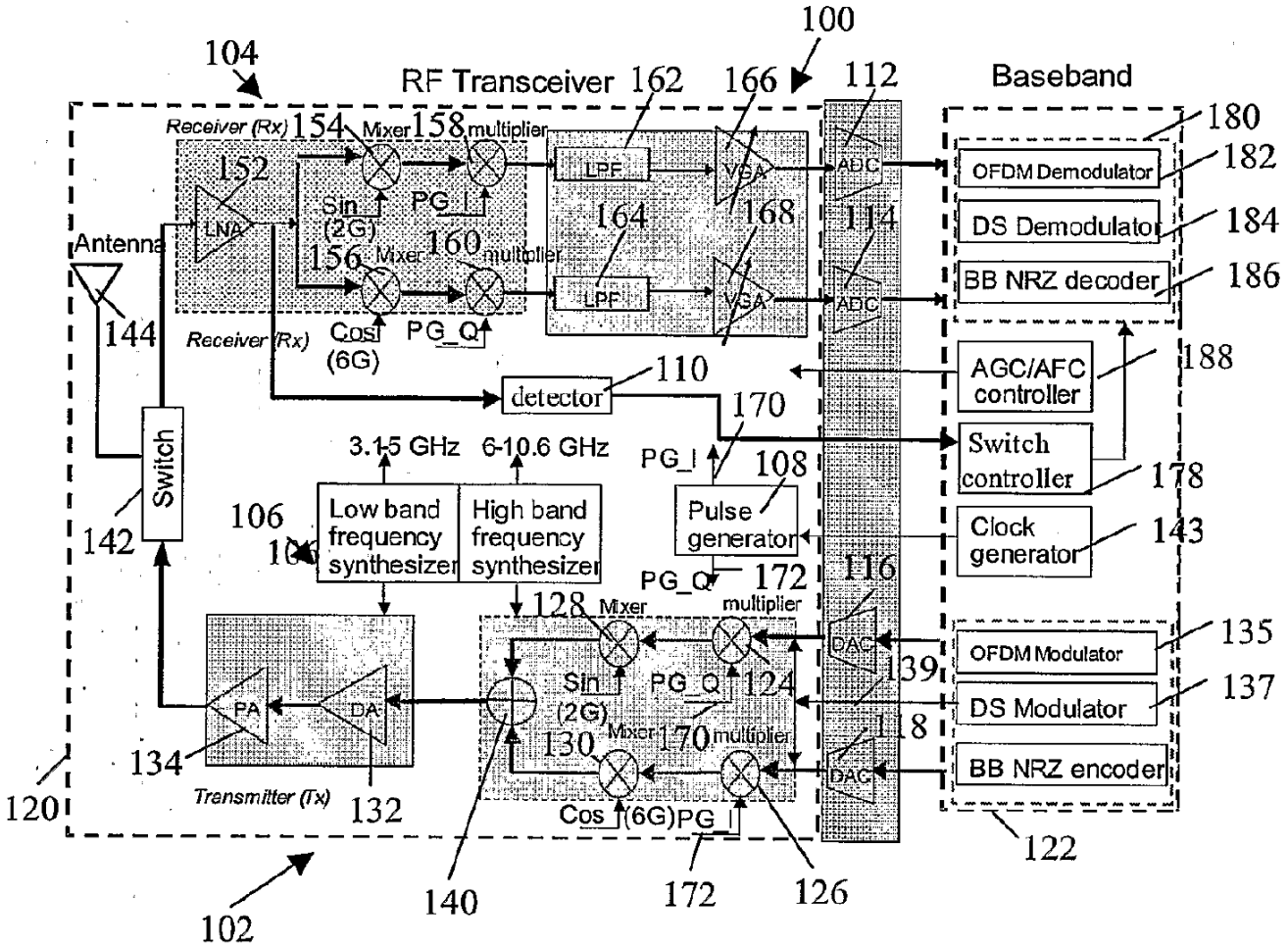


Figure 1

See, e.g., Zheng at Figure 1.

Claim 1 of the '802 Patent	Prior Art Reference – Zheng
	In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027].

Claim 1 of the '802 Patent	Prior Art Reference – Zheng
	The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5)

Claim 1 of the '802 Patent	Prior Art Reference – Zheng
	where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.

Claim 2 of the '802 Patent	Prior Art Reference – Zheng
[2.1] The method of claim 1	Zheng discloses all the elements of claim 1 for all the reasons provided above.
[2.2] wherein frequency difference between the first center frequency and the second center frequency is greater than the sum of one-half the first frequency range and one-half the second frequency range.	Zheng discloses "wherein frequency difference between the first center frequency and the second center frequency is greater than the sum of one-half the first frequency range and one-half the second frequency range." See, e.g.: In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design.

Claim 2 of the '802 Patent	Prior Art Reference – Zheng
	As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027]. The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029].

Claim 2 of the '802 Patent	Prior Art Reference – Zheng
	The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5) where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art.

Claim 2 of the '802 Patent	Prior Art Reference – Zheng
	Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.

Claim 3 of the '802 Patent	Prior Art Reference – Zheng
[3.1] The method of claim 1	Zheng discloses all the elements of claim 1 for all the reasons provided above.
[3.2] wherein the first and second information are transmitted using the same power amplifier in said wireless transmitter.	Zheng discloses "wherein the first and second information are transmitted using the same power amplifier in said wireless transmitter." See, e.g.:

Claim 3 of the '802 Patent	Prior Art Reference – Zheng

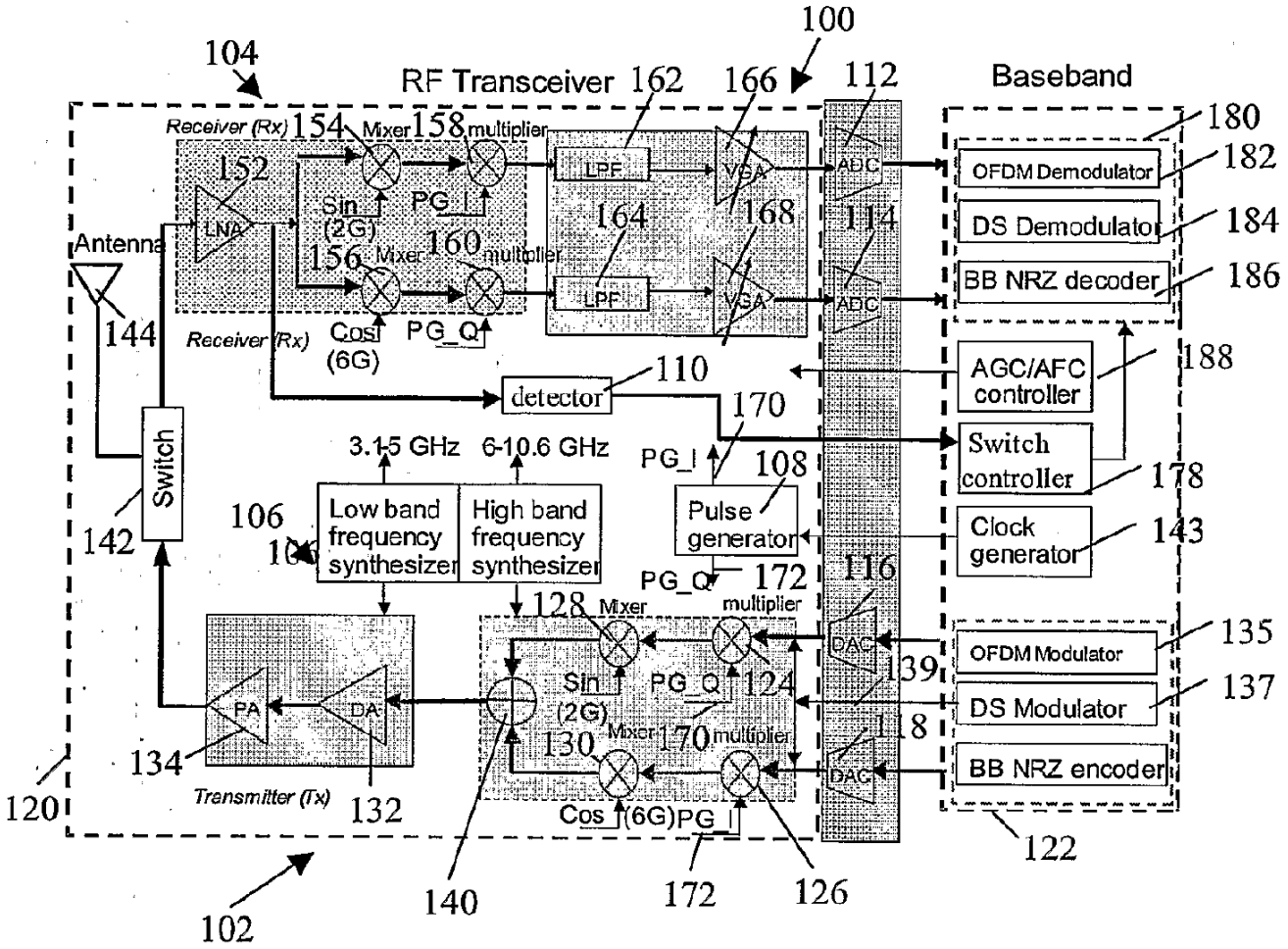


Figure 1

See, e.g., Zheng at Figure 1.

Claim 3 of the '802 Patent	Prior Art Reference – Zheng
	In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027].

Claim 3 of the '802 Patent	Prior Art Reference – Zheng
	The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5)

Claim 3 of the '802 Patent	Prior Art Reference – Zheng
	where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.

Claim 4 of the '802 Patent	Prior Art Reference – Zheng
[4.1] The method of claim 3	Zheng discloses all the elements of claim 3 for all the reasons provided above.
[4.2] wherein the bandwidth of said power amplifier is greater than the difference between the first lowest frequency and the second highest frequency.	Zheng discloses "wherein the bandwidth of said power amplifier is greater than the difference between the first lowest frequency and the second highest frequency." See, e.g.: In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters

Claim 4 of the '802 Patent	Prior Art Reference – Zheng
	(ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027]. The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the

Claim 4 of the '802 Patent	Prior Art Reference – Zheng
	different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5) where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further

Claim 4 of the '802 Patent	Prior Art Reference – Zheng
	motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.

Claim 6 of the '802 Patent	Prior Art Reference – Zheng
[6.1] The method of claim 1	Zheng discloses all the elements of claim 1 for all the reasons provided above.
[6.2] wherein the first information corresponds to a first wireless protocol and the second information corresponds to a second wireless protocol.	Zheng discloses "wherein the first information corresponds to a first wireless protocol and the second information corresponds to a second wireless protocol." See, e.g.: In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be

Claim 6 of the '802 Patent	Prior Art Reference – Zheng
	upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027]. The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is

Claim 6 of the '802 Patent	Prior Art Reference – Zheng
	from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5) where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.

Claim 7 of the '802 Patent	Prior Art Reference – Zheng
[7.1] The method of claim 1	Zheng discloses all the elements of claim 1 for all the reasons provided above.
[7.2] wherein the first information and the second information are the same data transmitted across two different frequencies.	Zheng discloses "wherein the first information and the second information are the same data transmitted across two different frequencies." See, e.g.: In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading

Claim 7 of the '802 Patent	Prior Art Reference – Zheng
	and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027]. The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156

Claim 7 of the '802 Patent	Prior Art Reference – Zheng
	can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5) where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184.

Claim 7 of the '802 Patent	Prior Art Reference – Zheng
	See, e.g., Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.

Claim 8 of the '802 Patent	Prior Art Reference – Zheng
[8.1] The method of claim 1	Zheng discloses all the elements of claim 1 for all the reasons provided above.
[8.2] wherein the first information and the second information are from the same data stream.	Zheng discloses "wherein the first information and the second information are from the same data stream." See, e.g.: In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122.

Claim 8 of the '802 Patent	Prior Art Reference – Zheng
	The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027]. The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below.

Claim 8 of the '802 Patent	Prior Art Reference – Zheng
	See, e.g., Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5) where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.

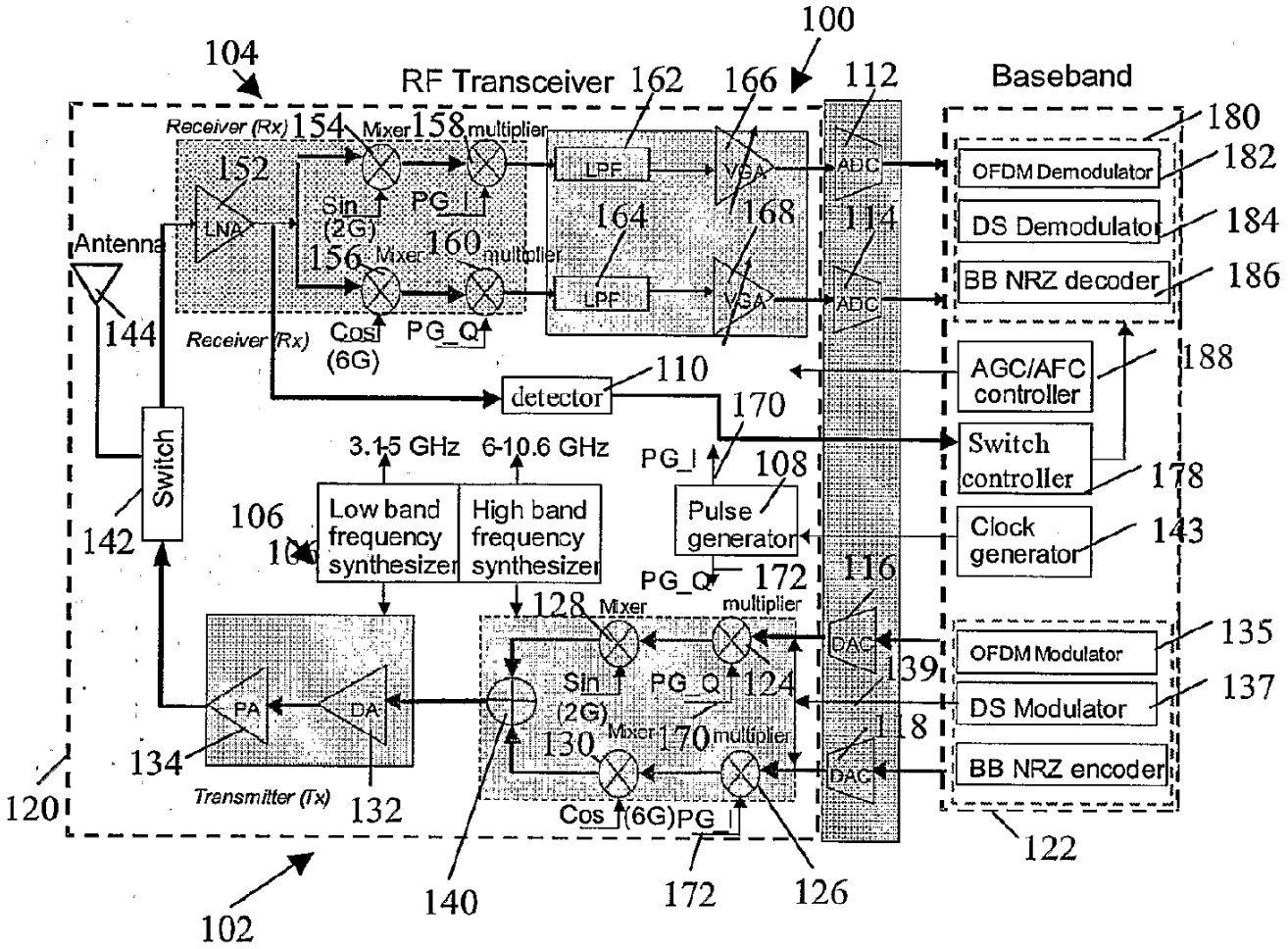
Claim 9 of the '802 Patent	Prior Art Reference – Zheng
[9.1] The method of claim 1	Zheng discloses all the elements of claim 1 for all the reasons provided above.
[9.2] wherein first information and second information comprise a plurality of OFDM symbols, wherein a first symbol is transmitted during a first time slot across the first frequency range and a second symbol is transmitted during the first time slot across the second frequency range, and wherein a third symbol is transmitted during a second time slot across the first frequency range and a fourth symbol is transmitted during the second time slot across a second frequency range.	Zheng discloses "wherein first information and second information comprise a plurality of OFDM symbols, wherein a first symbol is transmitted during a first time slot across the first frequency range and a second symbol is transmitted during the first time slot across the second frequency range, and wherein a third symbol is transmitted during a second time slot across the first frequency range and a fourth symbol is transmitted during the second time slot across a second frequency range." See, e.g.: In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency

Claim 9 of the '802 Patent	Prior Art Reference – Zheng
	upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027]. The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2.

Claim 9 of the '802 Patent	Prior Art Reference – Zheng
	In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5) where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.

Claim 10 of the '802 Patent	Prior Art Reference – Zheng
[10.1] A method of transmitting information in a wireless communication channel comprising:	To the extent the preamble is limiting, Zheng discloses "A method of transmitting information in a wireless communication channel comprising." See, e.g.:

Claim 10 of the '802 Patent	Prior Art Reference – Zheng



See, e.g., Zheng at Figure 1.

Claim 10 of the '802 Patent	Prior Art Reference – Zheng
	In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027].

Claim 10 of the '802 Patent	Prior Art Reference – Zheng
	Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.
[10.2] receiving a first digital signal comprising first data to be transmitted;	Zheng discloses "receiving a first digital signal comprising first data to be transmitted." See, e.g.:

Claim 10 of the '802 Patent	Prior Art Reference – Zheng

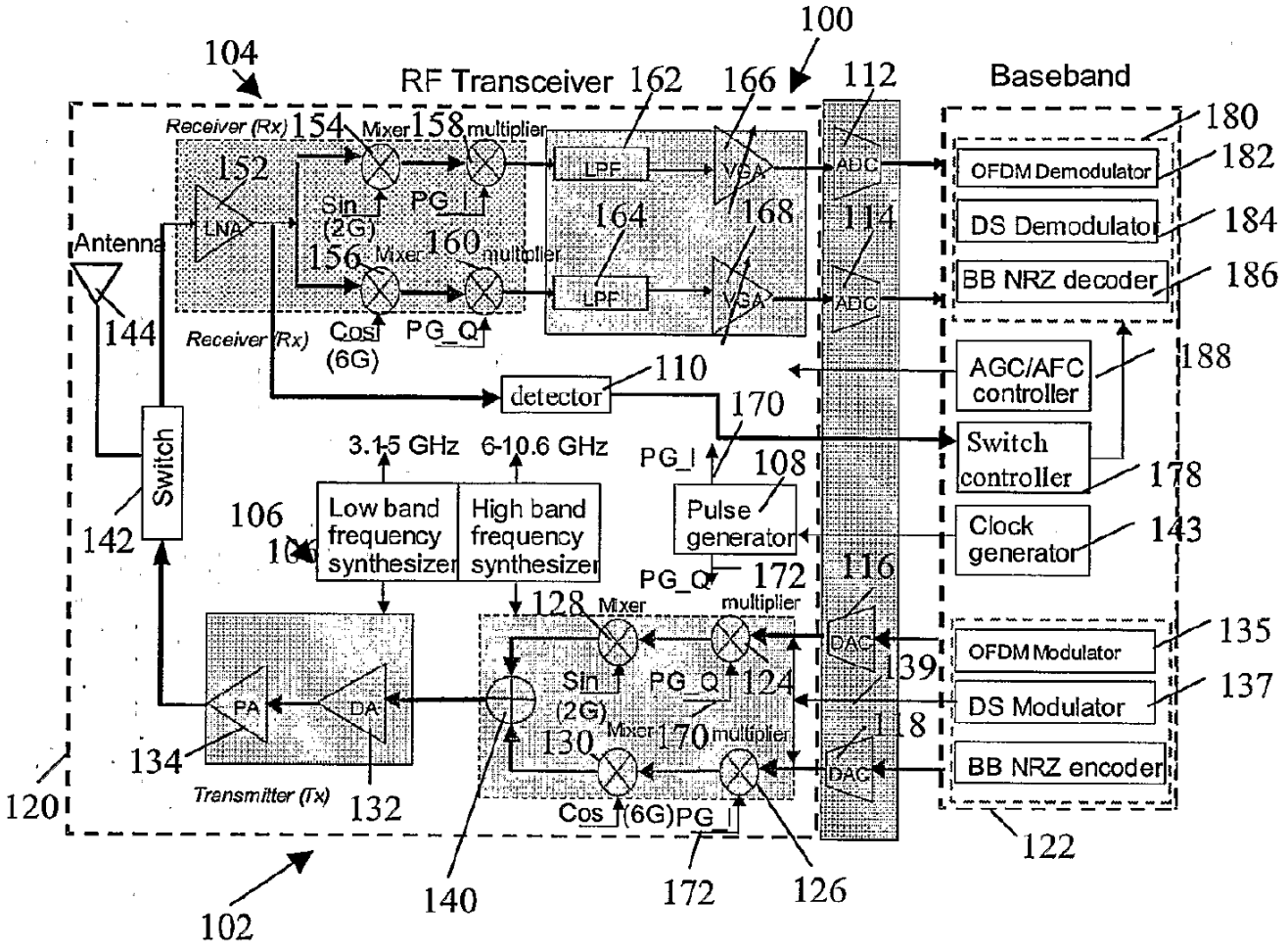


Figure 1

See, e.g., Zheng at Figure 1.

Claim 10 of the '802 Patent	Prior Art Reference – Zheng
	In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See*, *e.g.*, Zheng at ¶ [0024]-[0027].

Claim 10 of the '802 Patent	Prior Art Reference – Zheng
	The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5)

Claim 10 of the '802 Patent	Prior Art Reference – Zheng
	where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.
[10.3] receiving a second digital signal comprising second data to be transmitted;	Zheng discloses "receiving a second digital signal comprising second data to be transmitted." See, e.g.:

Claim 10 of the '802 Patent	Prior Art Reference – Zheng

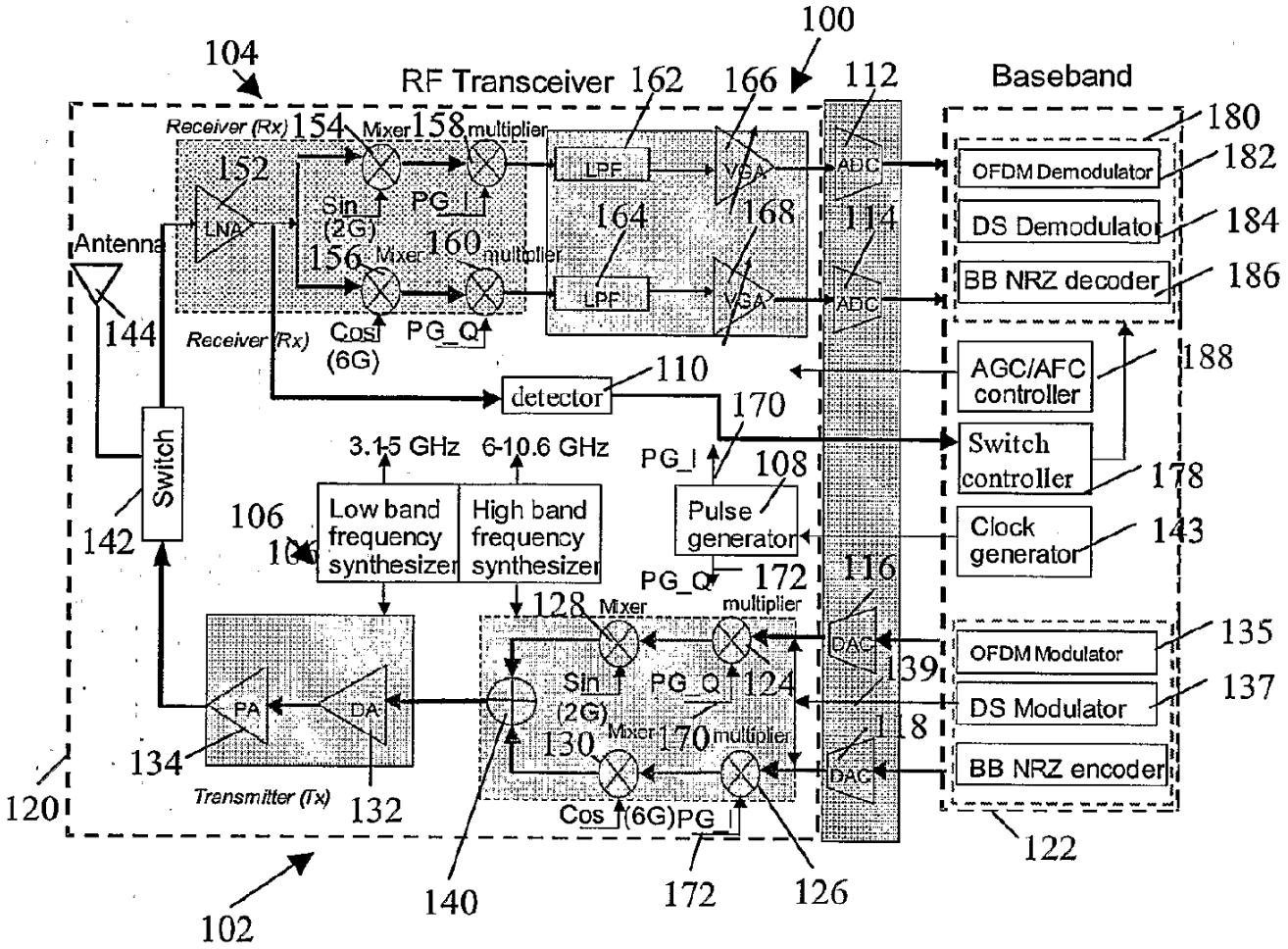


Figure 1

See, e.g., Zheng at Figure 1.

Claim 10 of the '802 Patent	Prior Art Reference – Zheng
	In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027].

Claim 10 of the '802 Patent	Prior Art Reference – Zheng
	The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5)

Claim 10 of the '802 Patent	Prior Art Reference – Zheng
	where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.
[10.4] converting the first digital signal into a first analog signal using a first digital-to-analog converter, the first analog signal carrying the first data across a first frequency range;.	Zheng discloses "converting the first digital signal into a first analog signal using a first digital-to-analog converter, the first analog signal carrying the first data across a first frequency range." See, e.g.:

Claim 10 of the '802 Patent	Prior Art Reference – Zheng

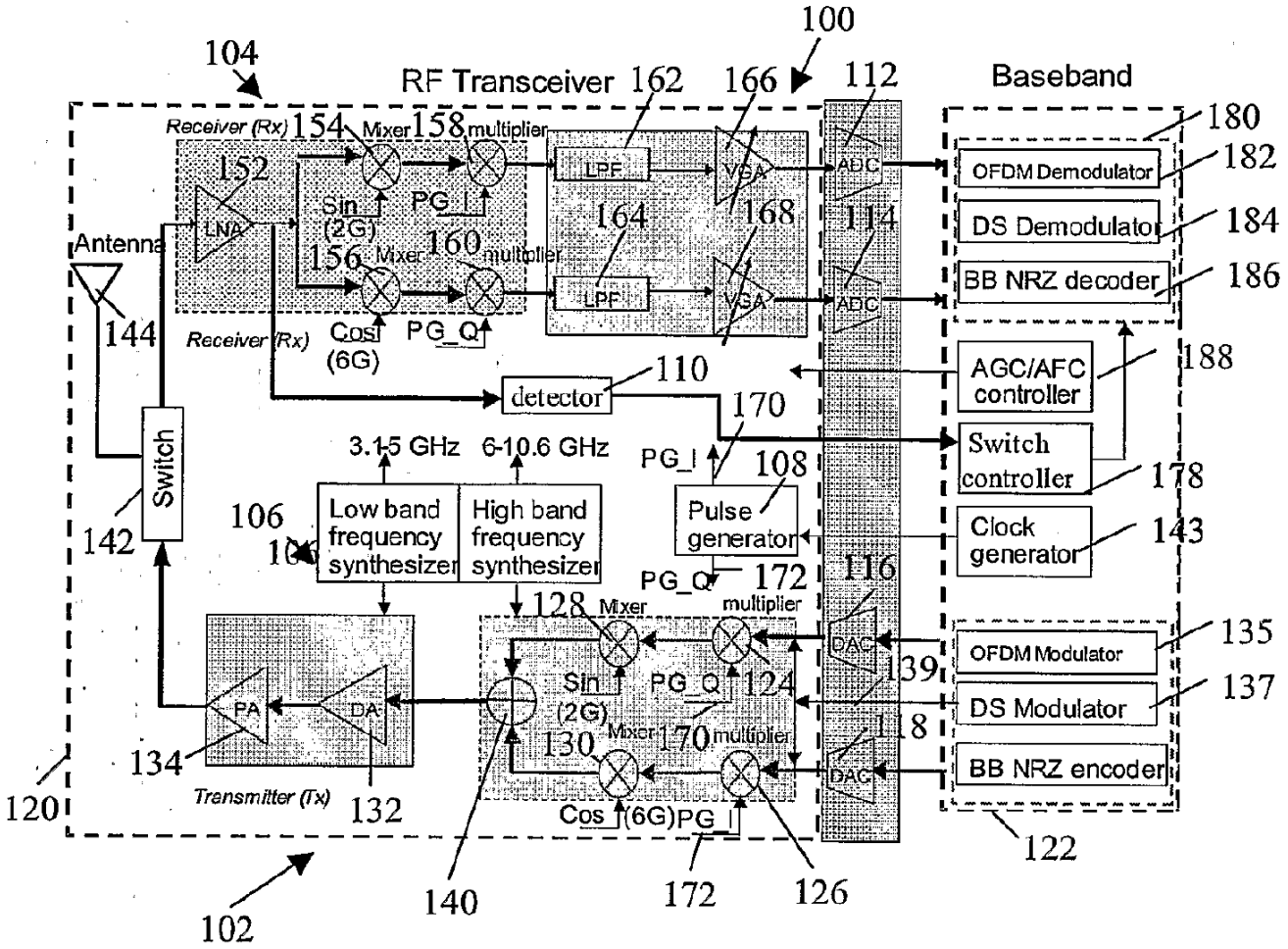


Figure 1

See, e.g., Zheng at Figure 1.

Claim 10 of the '802 Patent	Prior Art Reference – Zheng
	In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027].

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	The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5)

Claim 10 of the '802 Patent	Prior Art Reference – Zheng
	where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.
[10.5] converting the second digital signal into a second analog signal using a second digital-to-analog converter, the second analog signal carrying the second data across a second frequency range;	Zheng discloses "converting the second digital signal into a second analog signal using a second digital-to-analog converter, the second analog signal carrying the second data across a second frequency range." See, e.g.:

Claim 10 of the '802 Patent	Prior Art Reference – Zheng

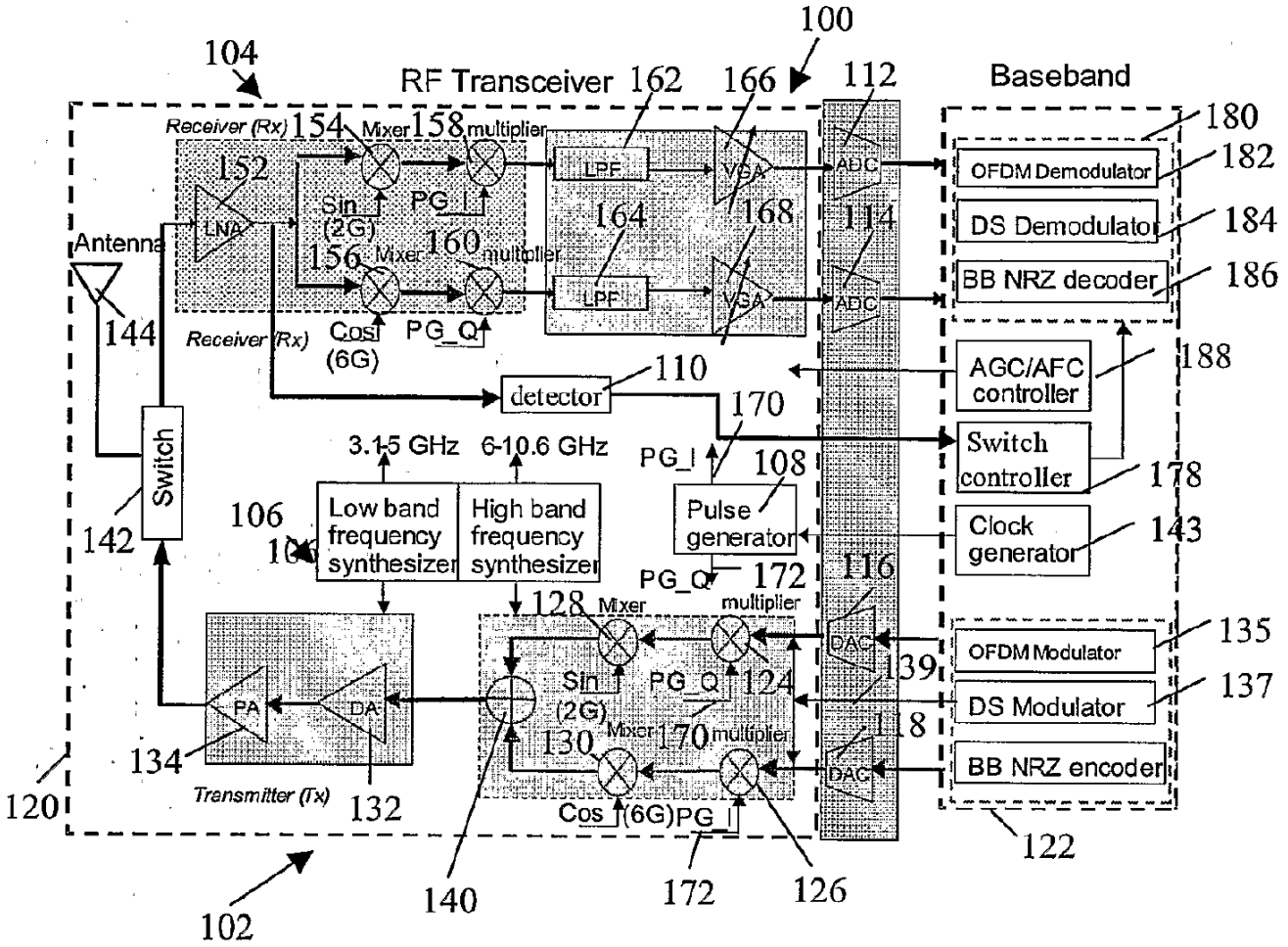

Figure 1

See, e.g., Zheng at Figure 1.

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	In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027].

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	The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5)

Claim 10 of the '802 Patent	Prior Art Reference – Zheng
	where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.
[10.6] up-converting the first analog signal to a first RF center frequency to produce a first up-converted analog signal, wherein the first up-converted analog signal comprises a first up-converted frequency range from the first RF center frequency minus one-half the first frequency range to the first RF center frequency plus one-half the first frequency range;	Zheng discloses "up-converting the first analog signal to a first RF center frequency to produce a first up-converted analog signal, wherein the first up-converted analog signal comprises a first up-converted frequency range from the first RF center frequency minus one-half the first frequency range to the first RF center frequency plus one-half the first frequency range." See, e.g.:

Claim 10 of the '802 Patent	Prior Art Reference – Zheng

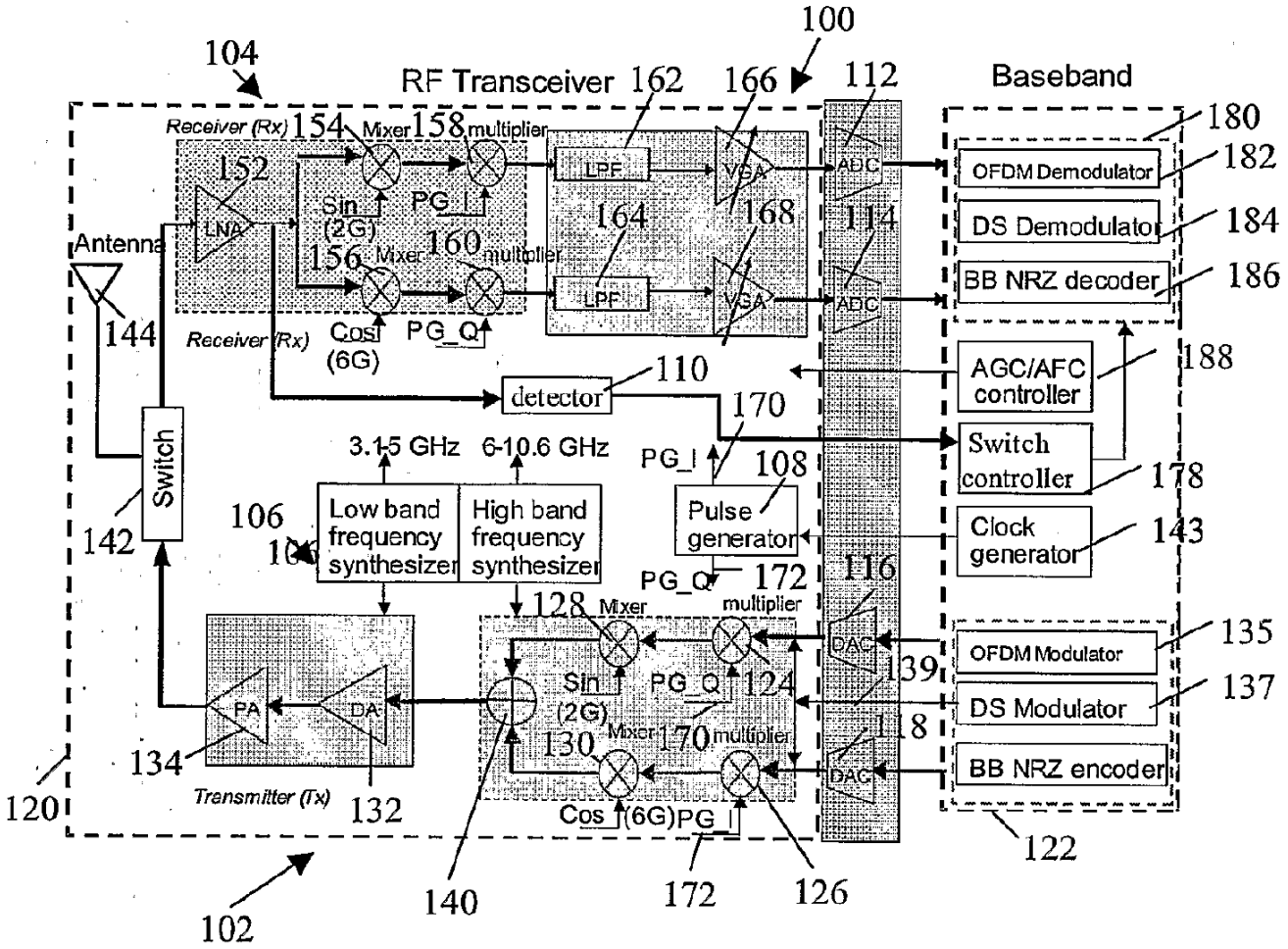

Figure 1

See, e.g., Zheng at Figure 1.

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	In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027].

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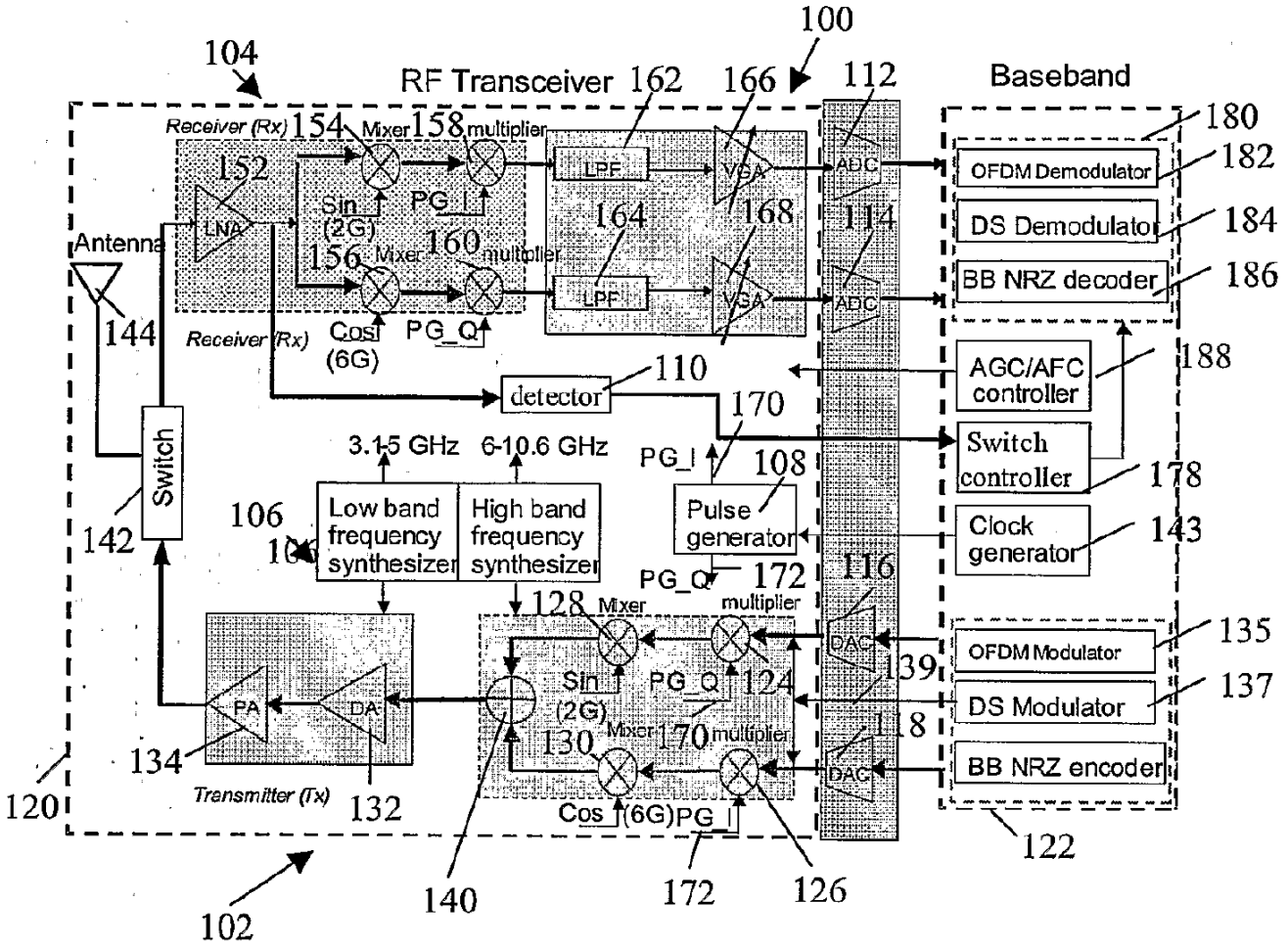
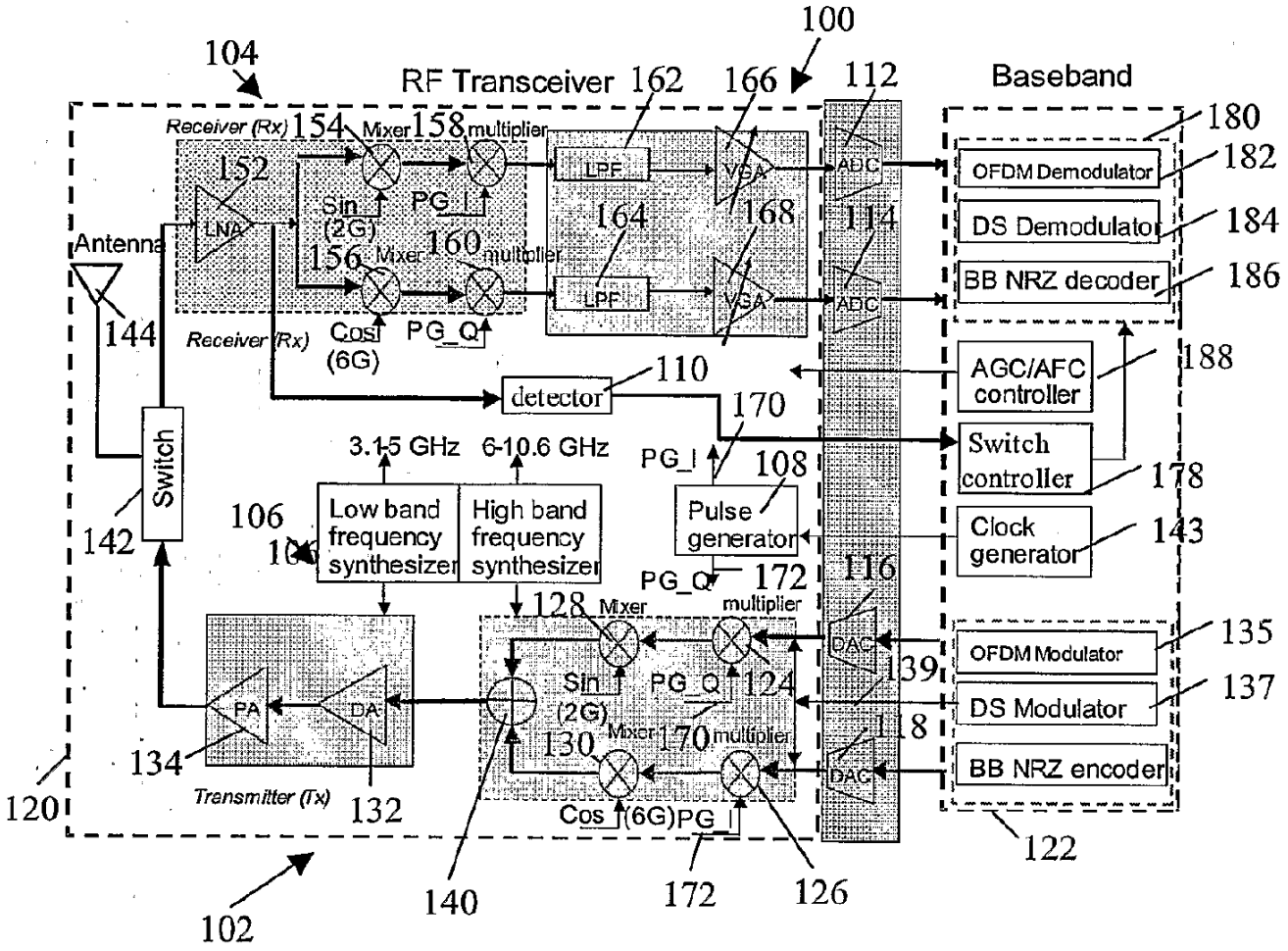
	where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.
[10.7] up-converting the second analog signal to a second RF center frequency greater than the first center RF frequency to produce a second up-converted analog signal, wherein the second up-converted analog signal comprises a second up-converted frequency range from the second RF center frequency minus one-half the second frequency range to the second RF center frequency plus one-half the second frequency range, and wherein a frequency difference between the first RF center	Zheng discloses "up-converting the second analog signal to a second RF center frequency greater than the first center RF frequency to produce a second up-converted analog signal, wherein the second up-converted analog signal comprises a second up-converted frequency range from the second RF center frequency minus one-half the second frequency range to the second RF center frequency plus one-half the second frequency range, and wherein a frequency difference between the first RF center frequency and the second RF center frequency is greater than the sum of one-half the first frequency range and one-half the second frequency range." See, e.g.:

Claim 10 of the '802 Patent	Prior Art Reference – Zheng
frequency and the second RF center frequency is greater than the sum of one-half the first frequency range and one-half the second frequency range;	 Figure 1 *See, e.g.*, Zheng at Figure 1.

Claim 10 of the '802 Patent	Prior Art Reference – Zheng
	In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027].

Claim 10 of the '802 Patent	Prior Art Reference – Zheng
	The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5)

Claim 10 of the '802 Patent	Prior Art Reference – Zheng
	where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.
[10.8] combining the first up-converted analog signal and the second up-converted analog signal to produce a combined up-converted signal;	Zheng discloses "combining the first up-converted analog signal and the second up-converted analog signal to produce a combined up-converted signal." See, e.g.:

Claim 10 of the '802 Patent	Prior Art Reference – Zheng
	 Figure 1 *See, e.g.*, Zheng at Figure 1.

Claim 10 of the '802 Patent	Prior Art Reference – Zheng
	In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027].

Claim 10 of the '802 Patent	Prior Art Reference – Zheng
	The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5)

Claim 10 of the '802 Patent	Prior Art Reference – Zheng
	where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.
[10.9] amplifying the combined up-converted signal in a power amplifier resulting in an amplified combined up-converted signal; and	Zheng discloses "amplifying the combined up-converted signal in a power amplifier resulting in an amplified combined up-converted signal." See, e.g.:

Claim 10 of the '802 Patent	Prior Art Reference – Zheng

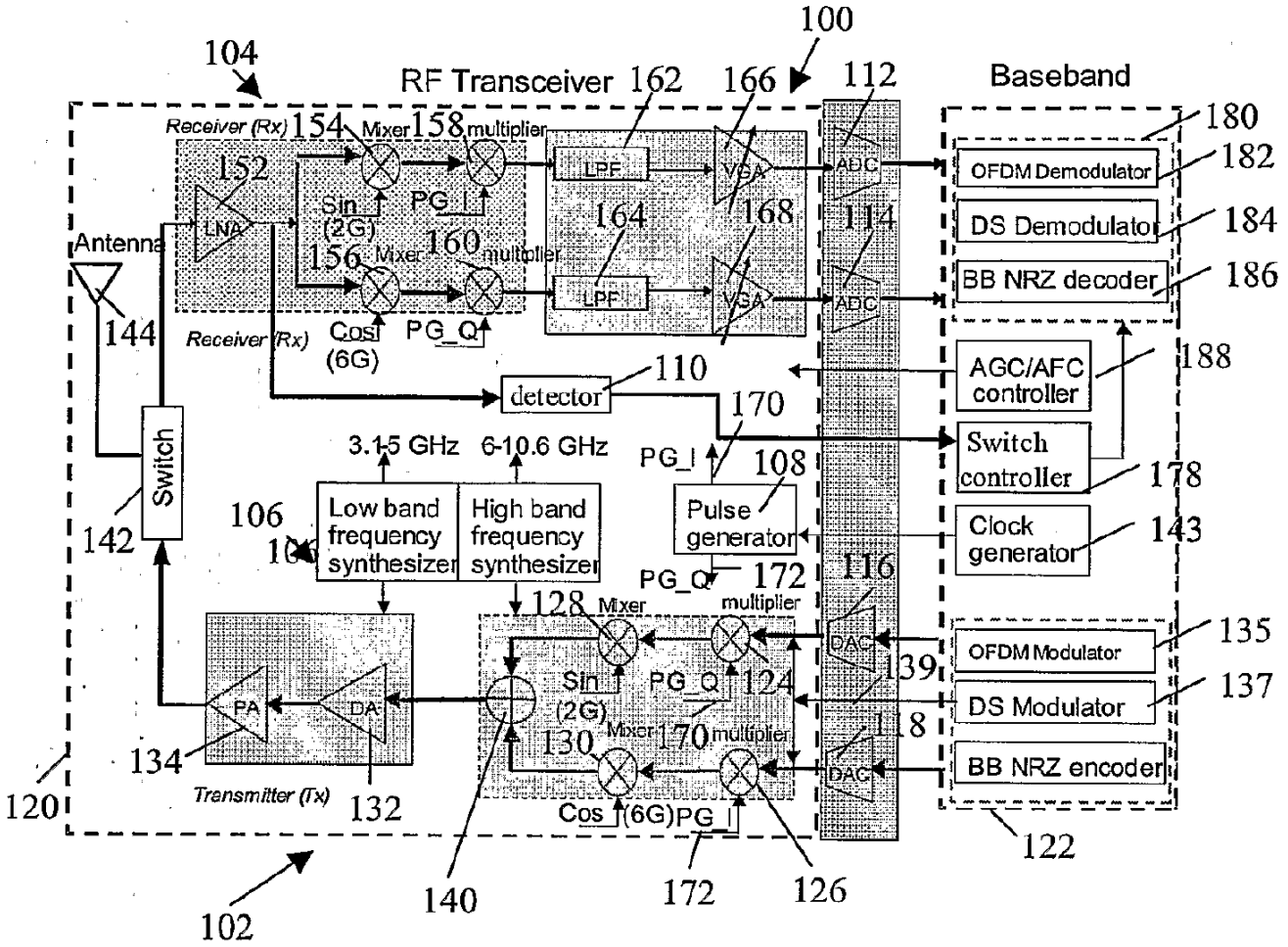


Figure 1

See, e.g., Zheng at Figure 1.

Claim 10 of the '802 Patent	Prior Art Reference – Zheng
	In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027].

Claim 10 of the '802 Patent	Prior Art Reference – Zheng
	The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5)

Claim 10 of the '802 Patent	Prior Art Reference – Zheng
	where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.
[10.10] transmitting the amplified combined up-converted signal on a first antenna,	Zheng discloses "transmitting the amplified combined up-converted signal on a first antenna." See, e.g.:

Claim 10 of the '802 Patent	Prior Art Reference – Zheng

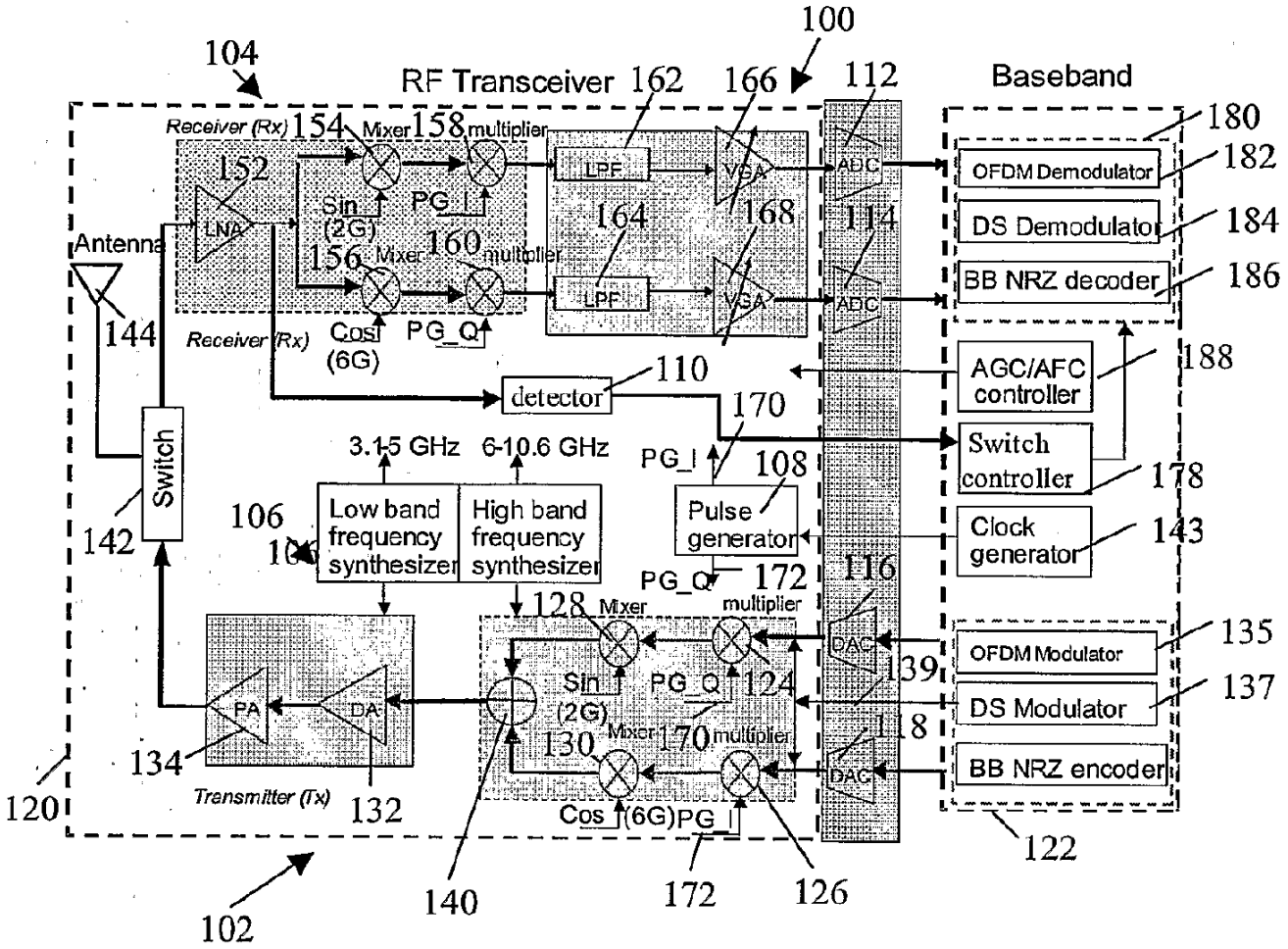


Figure 1

See, e.g., Zheng at Figure 1.

Claim 10 of the '802 Patent	Prior Art Reference – Zheng
	In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027].

Claim 10 of the '802 Patent	Prior Art Reference – Zheng
	The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5)

Claim 10 of the '802 Patent	Prior Art Reference – Zheng
	where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.
[10.11] wherein the bandwidth of said power amplifier is greater than the difference between a lowest frequency in the first up-converted frequency range and a highest frequency in the second up-converted frequency range.	Zheng discloses "wherein the bandwidth of said power amplifier is greater than the difference between a lowest frequency in the first up-converted frequency range and a highest frequency in the second up-converted frequency range." See, e.g.:

Claim 10 of the '802 Patent	Prior Art Reference – Zheng

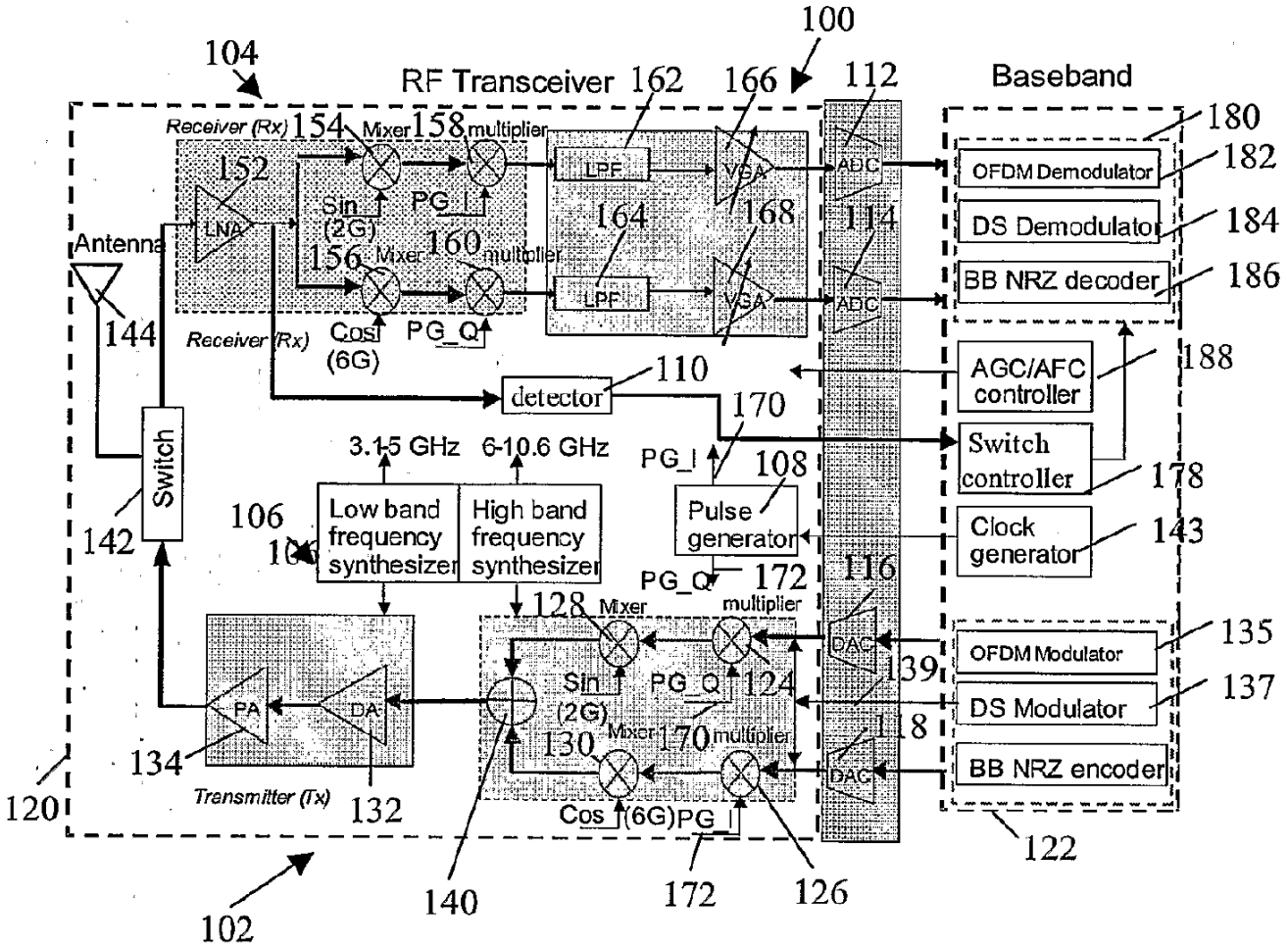


Figure 1

See, e.g., Zheng at Figure 1.

Claim 10 of the '802 Patent	Prior Art Reference – Zheng
	In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027].

Claim 10 of the '802 Patent	Prior Art Reference – Zheng
	The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5)

Claim 10 of the '802 Patent	Prior Art Reference – Zheng
	where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.

Claim 13 of the '802 Patent	Prior Art Reference – Zheng
[13.1] The method of claim 10	Zheng discloses all the elements of claim 10 for all the reasons provided above.
[13.2] wherein the first digital signal is encoded using a first wireless protocol and the second digital signal is encoded using a second wireless protocol.	Zheng discloses "wherein the first digital signal is encoded using a first wireless protocol and the second digital signal is encoded using a second wireless protocol." See, e.g.: In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters

Claim 13 of the '802 Patent	Prior Art Reference – Zheng
	(ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027]. The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the

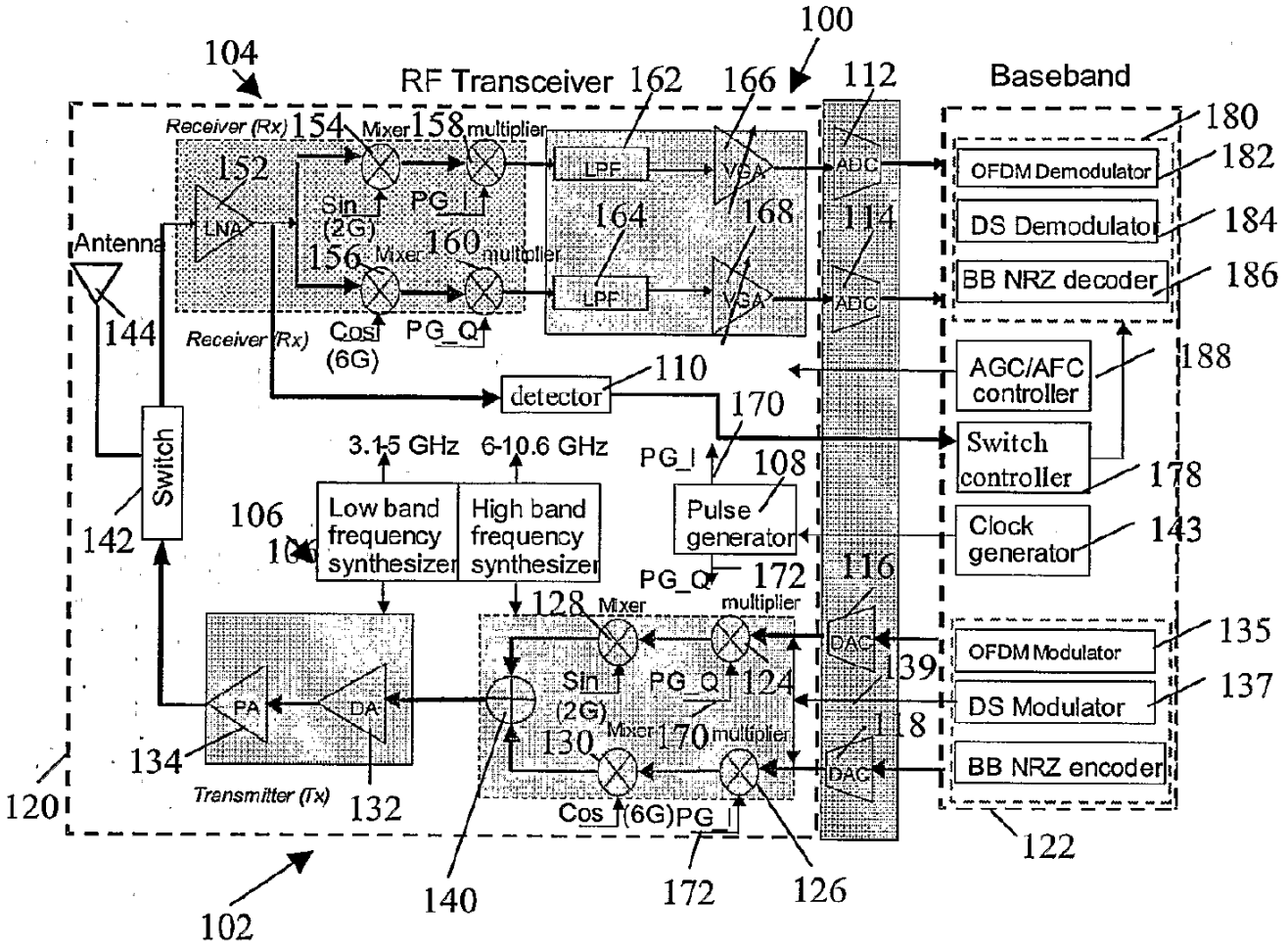
Claim 13 of the '802 Patent	Prior Art Reference – Zheng
	different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5) where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further

Claim 13 of the '802 Patent	Prior Art Reference – Zheng
	motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.

Claim 14 of the '802 Patent	Prior Art Reference – Zheng
[14.1] The method of claim 10	Zheng discloses all the elements of claim 10 for all the reasons provided above.
[14.2] wherein the second data is the same as the first data, the method further comprising:	Zheng discloses "wherein the second data is the same as the first data, the method further comprising." See, e.g.: In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be

Claim 14 of the '802 Patent	Prior Art Reference – Zheng
	upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027]. The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is

Claim 14 of the '802 Patent	Prior Art Reference – Zheng
	from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5) where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.
[14.3] receiving the transmitted signal on a second antenna;	Zheng discloses "receiving the transmitted signal on a second antenna." See, e.g.:

Claim 14 of the '802 Patent	Prior Art Reference – Zheng
	 Figure 1 *See, e.g.*, Zheng at Figure 1.

Claim 14 of the '802 Patent	Prior Art Reference – Zheng
	In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027].

Claim 14 of the '802 Patent	Prior Art Reference – Zheng
	The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5)

Claim 14 of the '802 Patent	Prior Art Reference – Zheng
	where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.
[14.4] amplifying the received signal in a low noise amplifier resulting in an amplified received up-converted signal, wherein the bandwidth of said low noise amplifier is greater than the difference between the lowest frequency in the first up-converted frequency range and the highest frequency in the second up-converted frequency range;	Zheng discloses "amplifying the received signal in a low noise amplifier resulting in an amplified received up-converted signal, wherein the bandwidth of said low noise amplifier is greater than the difference between the lowest frequency in the first up-converted frequency range and the highest frequency in the second up-converted frequency range." See, e.g.:

Claim 14 of the '802 Patent	Prior Art Reference – Zheng

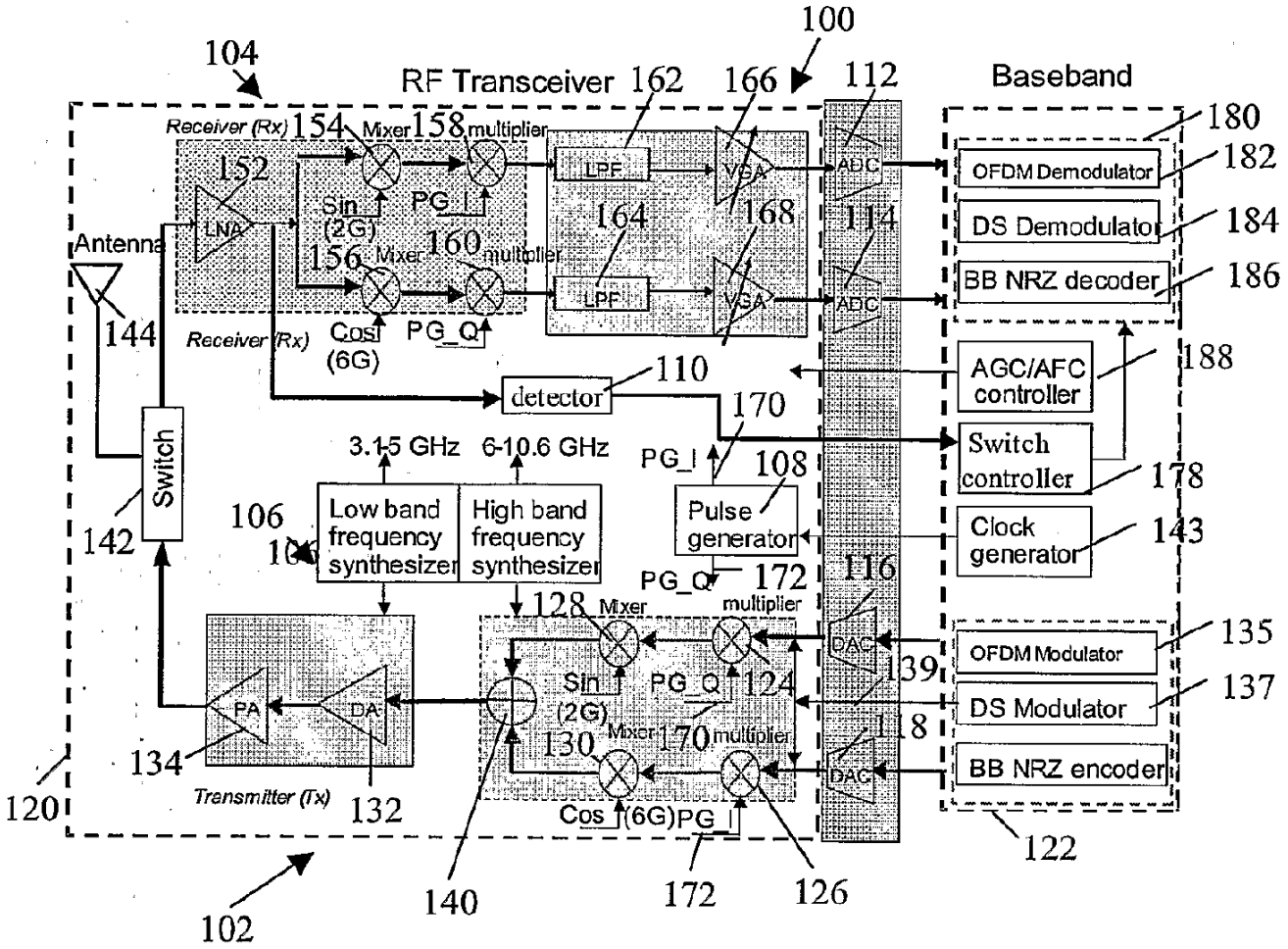


Figure 1

See, e.g., Zheng at Figure 1.

Claim 14 of the '802 Patent	Prior Art Reference – Zheng
	In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027].

Claim 14 of the '802 Patent	Prior Art Reference – Zheng
	The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5)

Claim 14 of the '802 Patent	Prior Art Reference – Zheng
	where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.
[14.5] down-converting the amplified received up-converted signal using a first down-converter and a signal corresponding to the first RF center frequency to produce a fourth analog signal corresponding to the first analog signal; and	Zheng discloses "down-converting the amplified received up-converted signal using a first down-converter and a signal corresponding to the first RF center frequency to produce a fourth analog signal corresponding to the first analog signal." See, e.g.:

Claim 14 of the '802 Patent	Prior Art Reference – Zheng

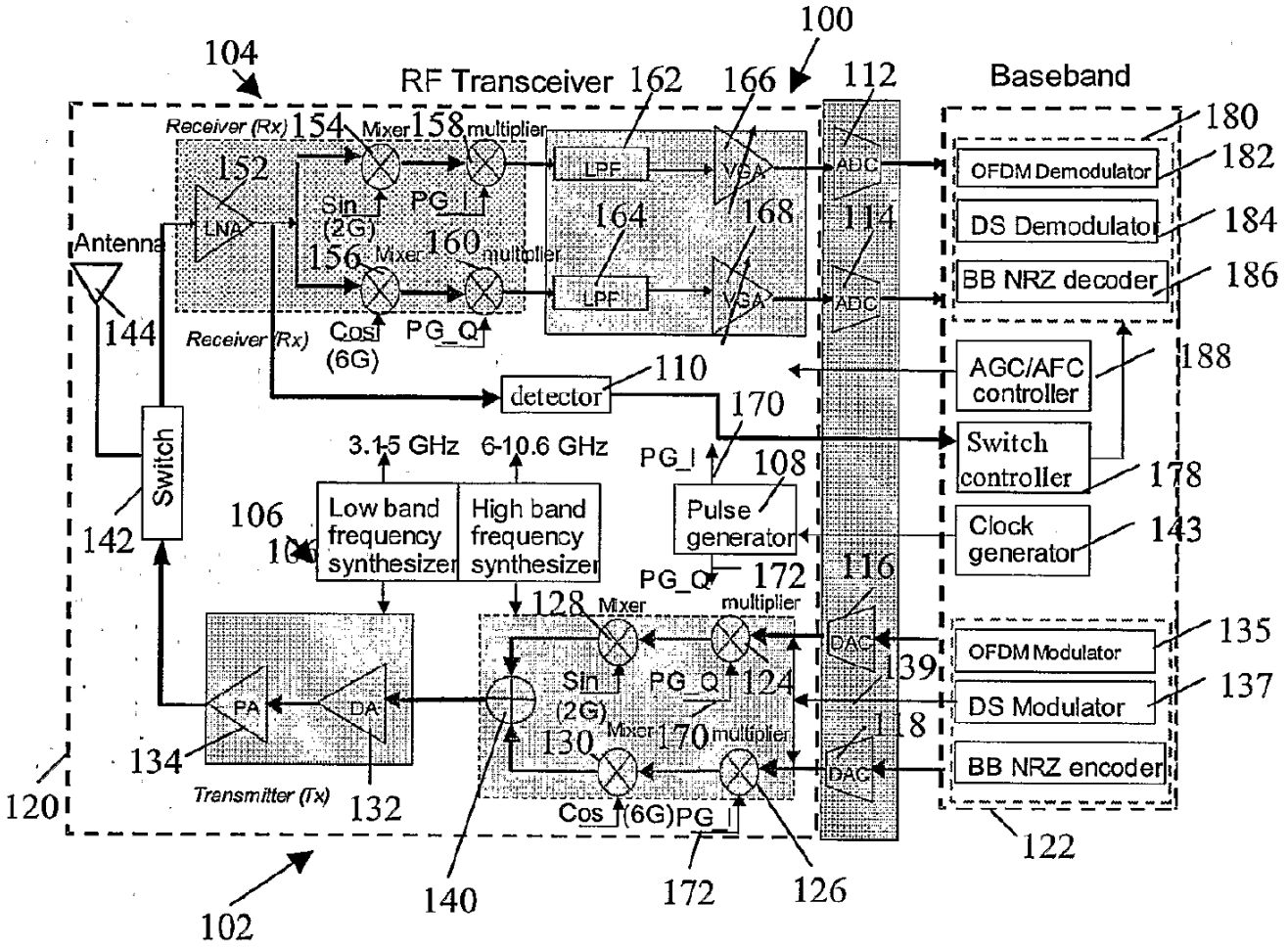


Figure 1

See, e.g., Zheng at Figure 1.

Claim 14 of the '802 Patent	Prior Art Reference – Zheng
	In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027].

Claim 14 of the '802 Patent	Prior Art Reference – Zheng
	The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5)

Claim 14 of the '802 Patent	Prior Art Reference – Zheng
	where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.
[14.6] down-converting the amplified received up-converted analog signal using a second down-converter and a signal corresponding to the second RF center frequency to produce a fifth analog signal corresponding to the second analog signal.	Zheng discloses "down-converting the amplified received up-converted analog signal using a second down-converter and a signal corresponding to the second RF center frequency to produce a fifth analog signal corresponding to the second analog signal." See, e.g.:

Claim 14 of the '802 Patent	Prior Art Reference – Zheng

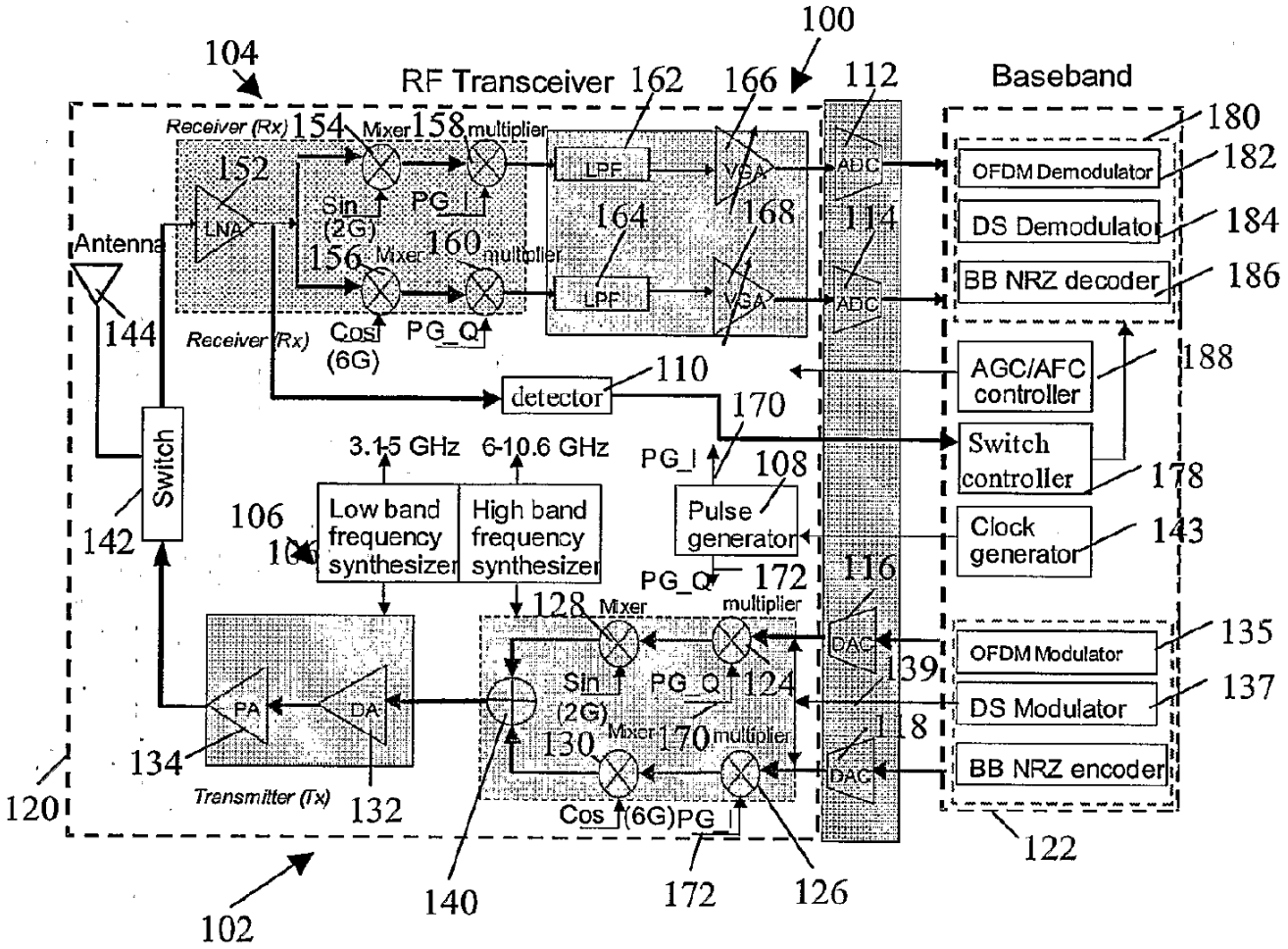


Figure 1

See, e.g., Zheng at Figure 1.

Claim 14 of the '802 Patent	Prior Art Reference – Zheng
	In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027].

Claim 14 of the '802 Patent	Prior Art Reference – Zheng
	The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5)

Claim 14 of the '802 Patent	Prior Art Reference – Zheng
	where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.

Claim 17 of the '802 Patent	Prior Art Reference – Zheng
[17.1] A wireless communication system comprising:	To the extent the preamble is limiting, Zheng discloses "A wireless communication system comprising." See, e.g.:

Claim 17 of the '802 Patent	Prior Art Reference – Zheng

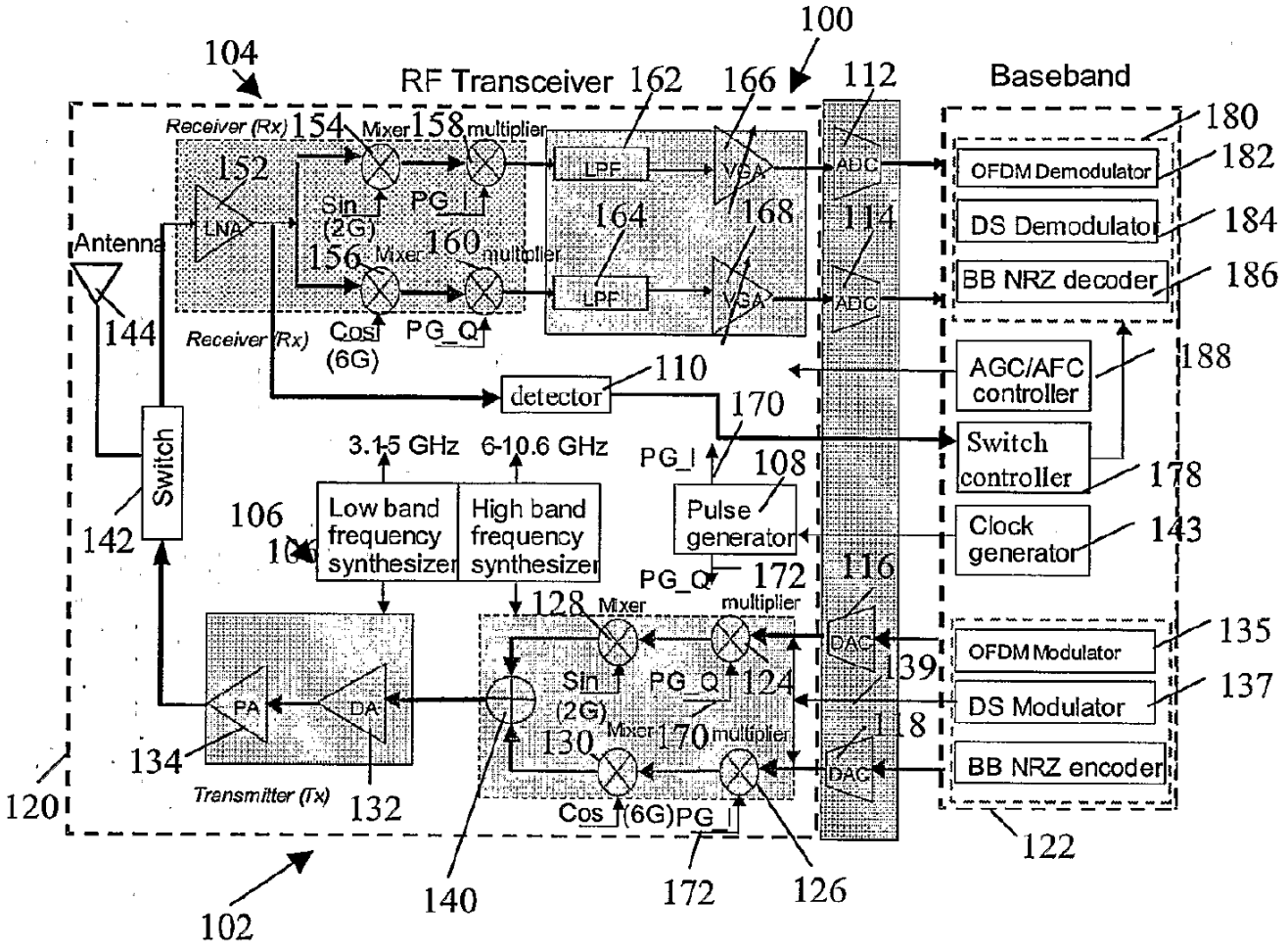


Figure 1

See, e.g., Zheng at Figure 1.

Claim 17 of the '802 Patent	Prior Art Reference – Zheng
	In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027].

Claim 17 of the '802 Patent	Prior Art Reference – Zheng
	Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.
[17.2] a baseband digital system for providing a first digital signal comprising a first data to be transmitted and a second digital signal comprising a second data to be transmitted;	Zheng discloses "a baseband digital system for providing a first digital signal comprising a first data to be transmitted and a second digital signal comprising a second data to be transmitted." See, e.g.:

Claim 17 of the '802 Patent	Prior Art Reference – Zheng

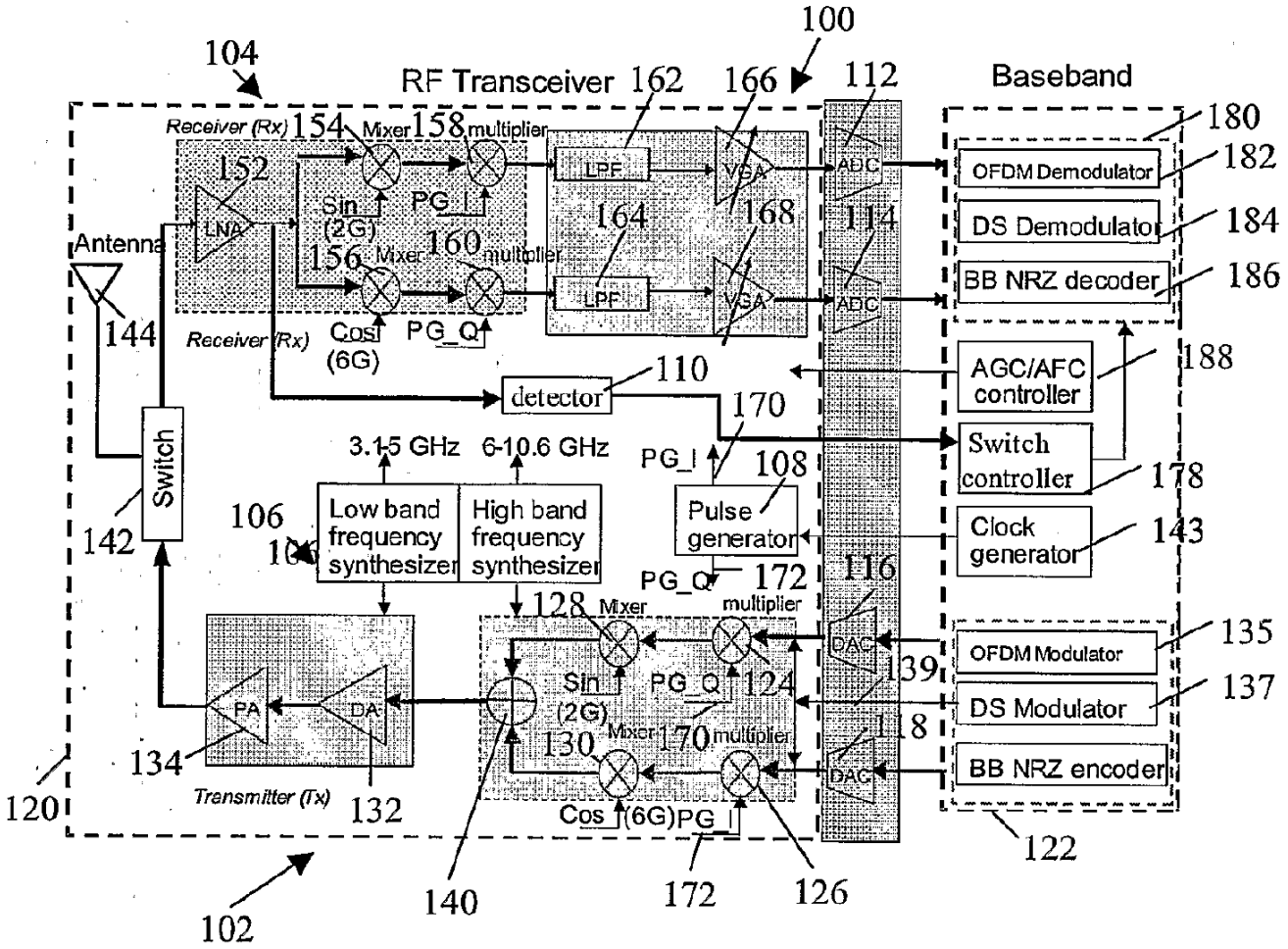


Figure 1

See, e.g., Zheng at Figure 1.

Claim 17 of the '802 Patent	Prior Art Reference – Zheng
	In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027].

Claim 17 of the '802 Patent	Prior Art Reference – Zheng
	The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5)

Claim 17 of the '802 Patent	Prior Art Reference – Zheng
	where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.
[17.3] a first digital-to-analog converter for receiving the first digital signal and converting the first digital signal into a first analog signal, the first analog signal carrying the first data across a first frequency range;	Zheng discloses "a first digital-to-analog converter for receiving the first digital signal and converting the first digital signal into a first analog signal, the first analog signal carrying the first data across a first frequency range." See, e.g.:

Claim 17 of the '802 Patent	Prior Art Reference – Zheng

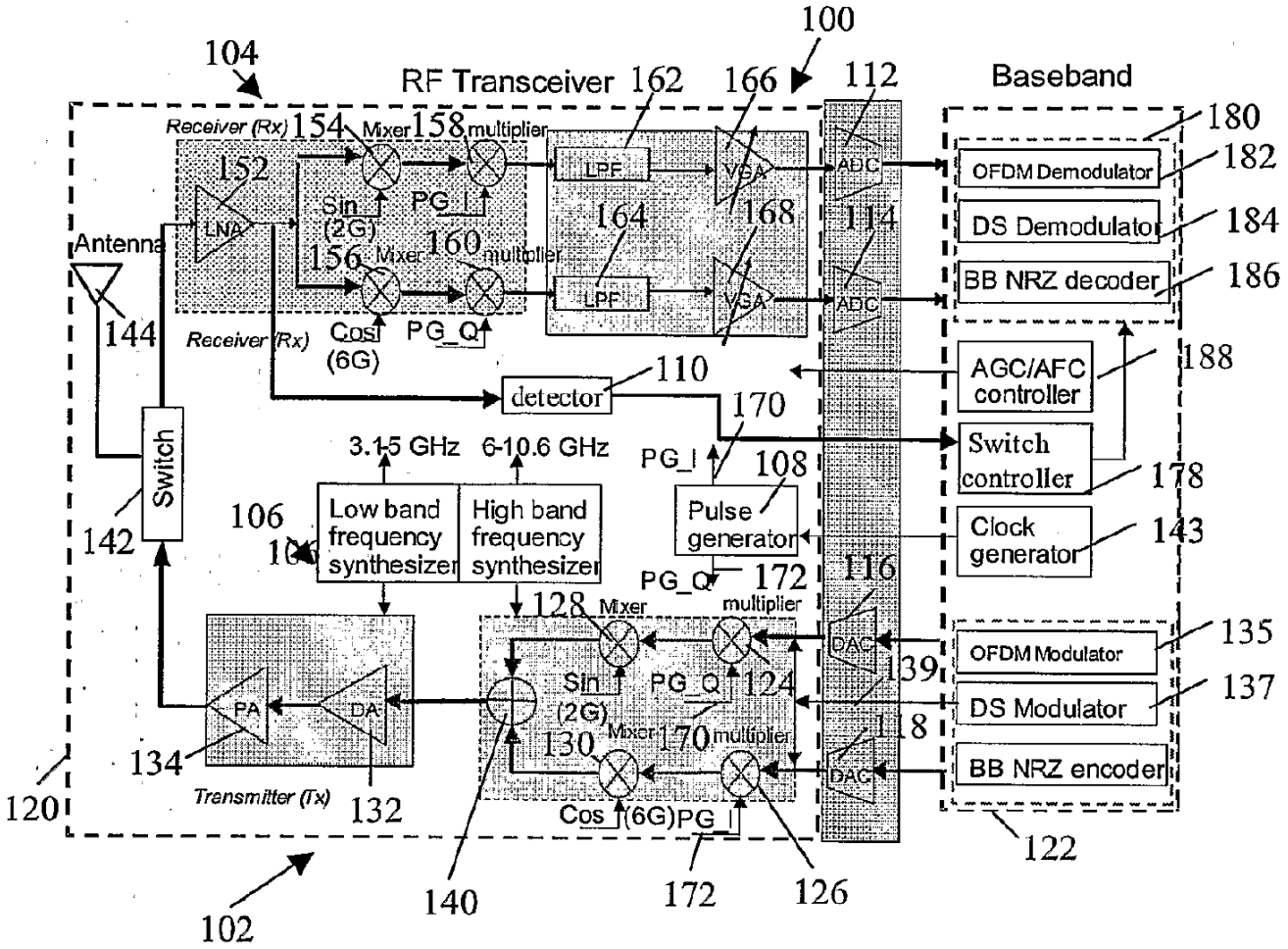


Figure 1

See, e.g., Zheng at Figure 1.

Claim 17 of the '802 Patent	Prior Art Reference – Zheng
	In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027].

Claim 17 of the '802 Patent	Prior Art Reference – Zheng
	The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5)

Claim 17 of the '802 Patent	Prior Art Reference – Zheng
	where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.
[17.4] a second digital-to-analog converter for receiving the second digital signal and converting the second digital signal into a second analog signal, the second analog signal carrying the second data across a second frequency range;	Zheng discloses "a second digital-to-analog converter for receiving the second digital signal and converting the second digital signal into a second analog signal, the second analog signal carrying the second data across a second frequency range." See, e.g.:

Claim 17 of the '802 Patent	Prior Art Reference – Zheng

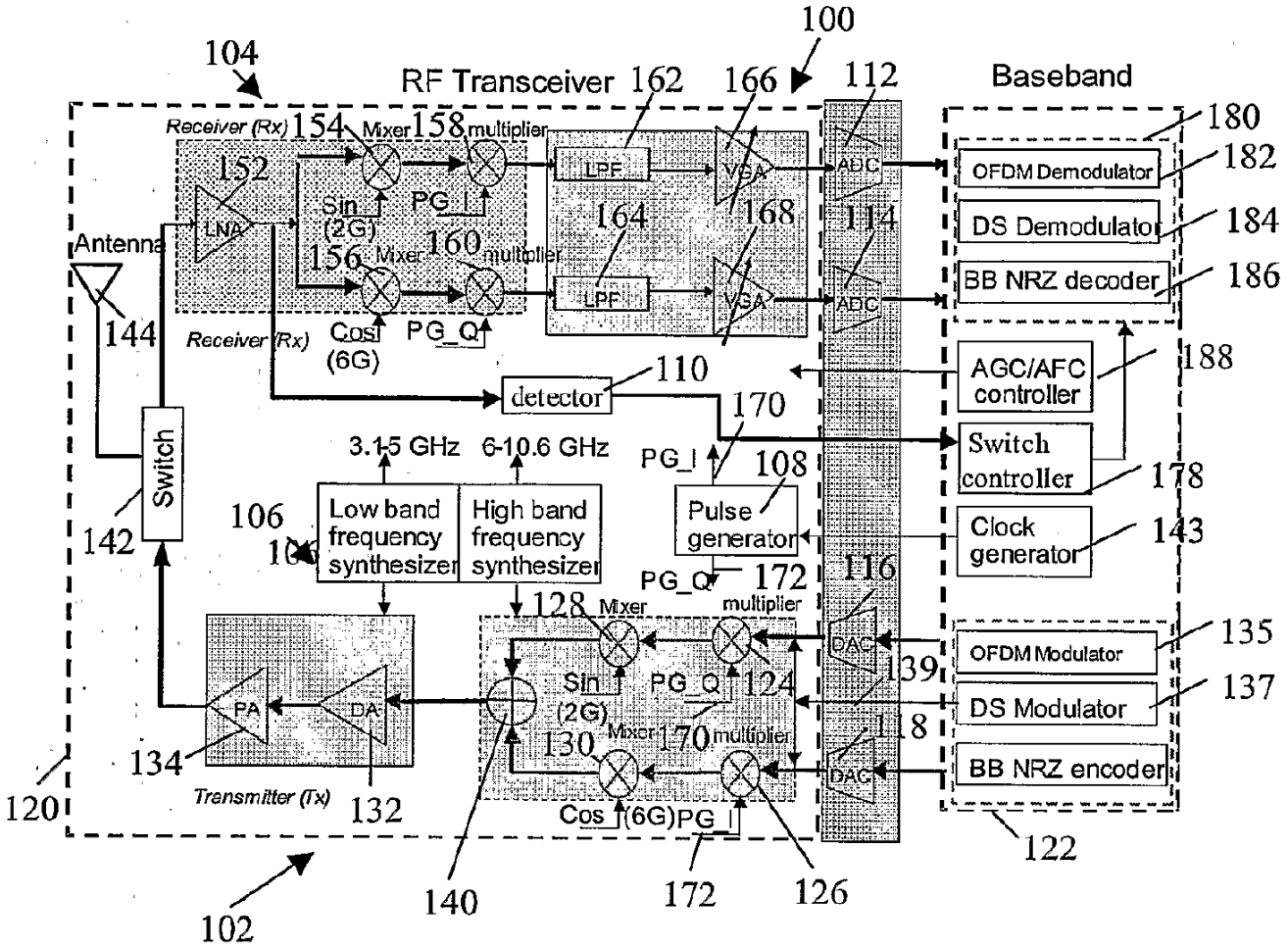


Figure 1

See, e.g., Zheng at Figure 1.

Claim 17 of the '802 Patent	Prior Art Reference – Zheng
	In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027].

Claim 17 of the '802 Patent	Prior Art Reference – Zheng
	The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5)

Claim 17 of the '802 Patent	Prior Art Reference – Zheng
	where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.
[17.5] a first up-converter circuit having a first input coupled to receive the first analog signal and a second input coupled to receive a first modulation signal having a first RF frequency, wherein the first up-converter outputs a first up-converted analog signal comprising a first up-converted frequency range from the first RF frequency minus one-half the first frequency range to the first RF frequency plus one-half the first frequency range;	Zheng discloses "a first up-converter circuit having a first input coupled to receive the first analog signal and a second input coupled to receive a first modulation signal having a first RF frequency, wherein the first up-converter outputs a first up-converted analog signal comprising a first up-converted frequency range from the first RF frequency minus one-half the first frequency range to the first RF frequency plus one-half the first frequency range." See, e.g.:

Claim 17 of the '802 Patent	Prior Art Reference – Zheng

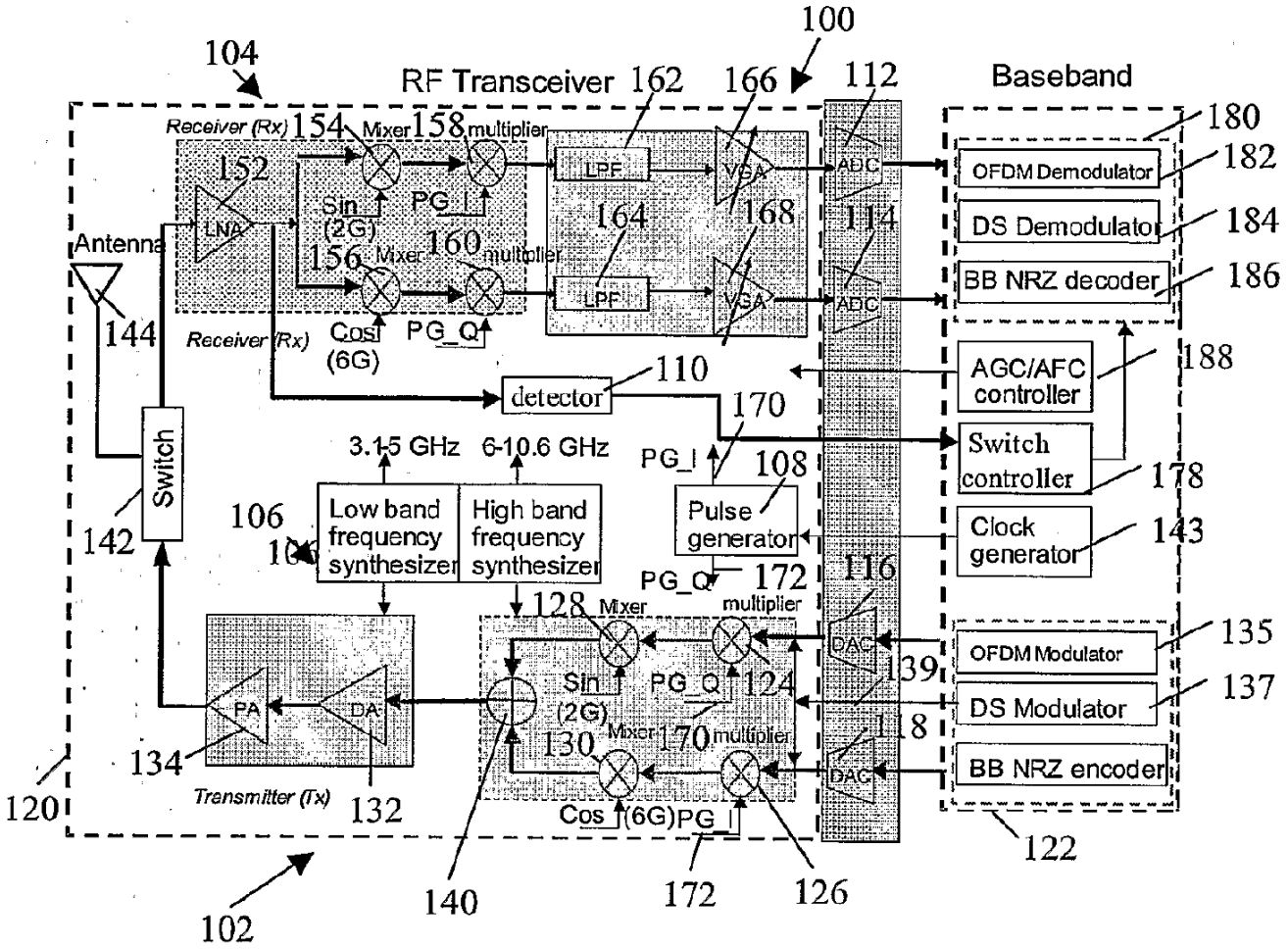


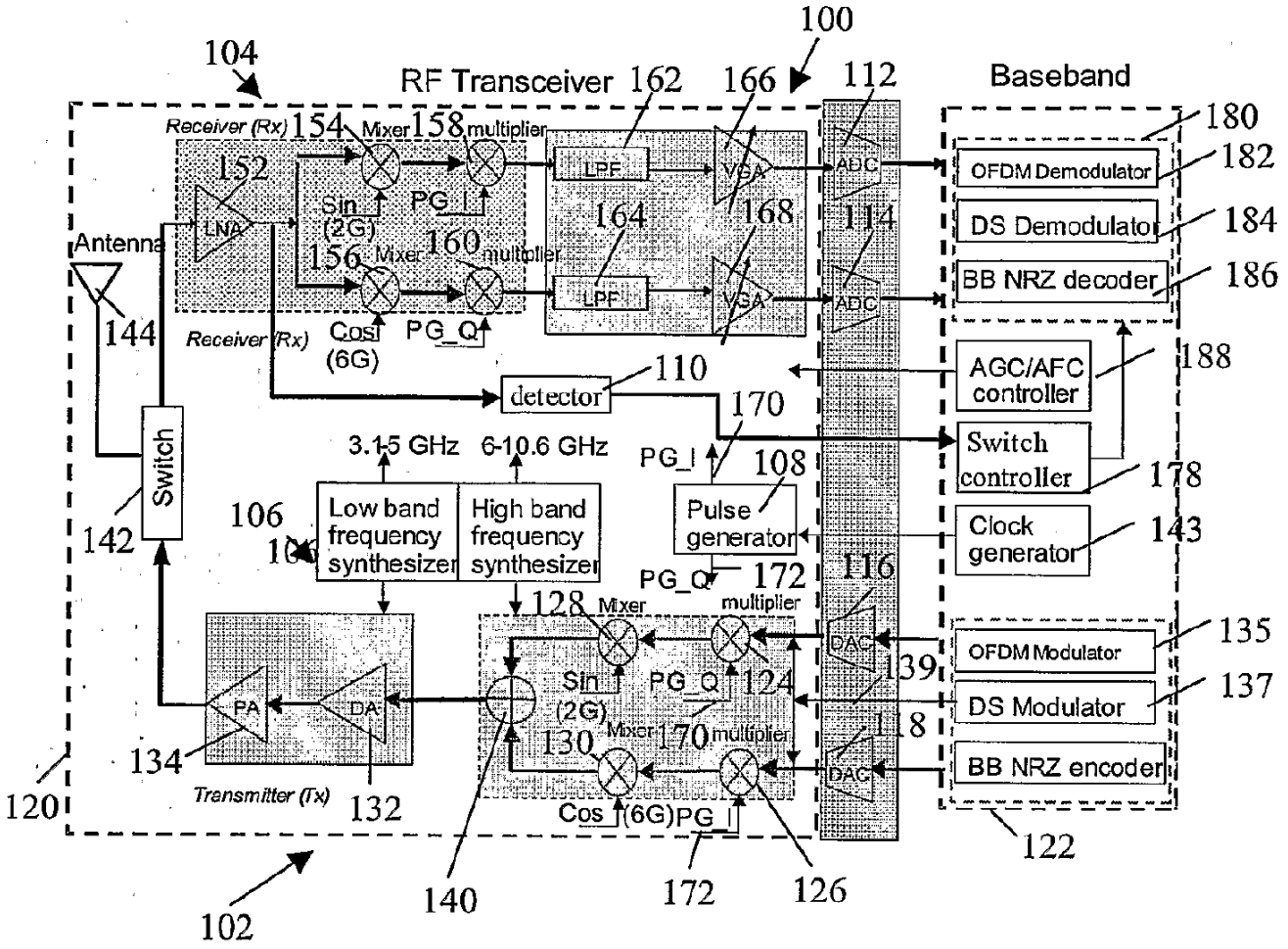
Figure 1

See, e.g., Zheng at Figure 1.

Claim 17 of the '802 Patent	Prior Art Reference – Zheng
	In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027].

Claim 17 of the '802 Patent	Prior Art Reference – Zheng
	The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5)

Claim 17 of the '802 Patent	Prior Art Reference – Zheng
	where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.
[17.6] a second up-converter circuit having a first input coupled to receive the second analog signal and a second input coupled to receive a second modulation signal having a second RF frequency, wherein the second up-converter outputs a second up-converted analog signal comprising a second up-converted frequency range from the second RF frequency minus one-half the second frequency range to the second RF frequency plus one-half the second frequency range, and wherein frequency	Zheng discloses "a second up-converter circuit having a first input coupled to receive the second analog signal and a second input coupled to receive a second modulation signal having a second RF frequency, wherein the second up-converter outputs a second up-converted analog signal comprising a second up-converted frequency range from the second RF frequency minus one-half the second frequency range to the second RF frequency plus one-half the second frequency range, and wherein frequency difference between the first RF frequency and the second RF frequency is greater than the sum of one-half the first frequency range and one-half the second frequency range." See, e.g.:

Claim 17 of the '802 Patent	Prior Art Reference – Zheng
difference between the first RF frequency and the second RF frequency is greater than the sum of one-half the first frequency range and one-half the second frequency range; and	 Figure 1 *See, e.g.*, Zheng at Figure 1.

Claim 17 of the '802 Patent	Prior Art Reference – Zheng
	In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027].

Claim 17 of the '802 Patent	Prior Art Reference – Zheng
	The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5)

Claim 17 of the '802 Patent	Prior Art Reference – Zheng
	where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.
[17.7] a power amplifier coupled to receive the first and second up-converted analog signals, wherein the bandwidth of the power amplifier is greater than the difference between a lowest frequency in the first up-converted frequency range and a highest frequency in the second up-converted frequency range.	Zheng discloses "a power amplifier coupled to receive the first and second up-converted analog signals, wherein the bandwidth of the power amplifier is greater than the difference between a lowest frequency in the first up-converted frequency range and a highest frequency in the second up-converted frequency range." See, e.g.:

Claim 17 of the '802 Patent	Prior Art Reference – Zheng

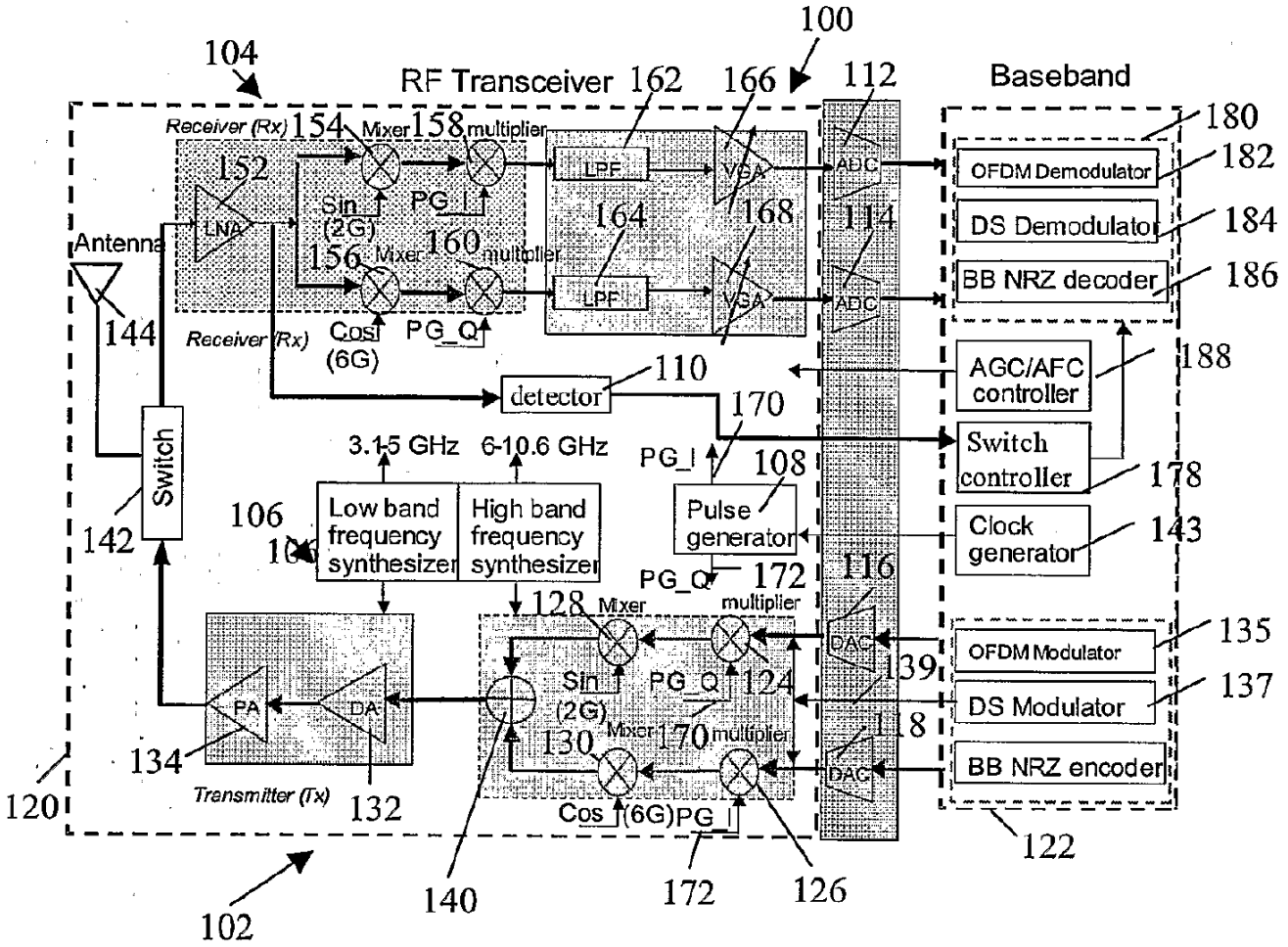


Figure 1

See, e.g., Zheng at Figure 1.

Claim 17 of the '802 Patent	Prior Art Reference – Zheng
	In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027].

Claim 17 of the '802 Patent	Prior Art Reference – Zheng
	The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5)

Claim 17 of the '802 Patent	Prior Art Reference – Zheng
	where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.

Claim 21 of the '802 Patent	Prior Art Reference – Zheng
[21.1] The communication system of claim 17	Zheng discloses all the elements of claim 17 for all the reasons provided above.
[21.2] wherein the first data of the first digital signal is encoded using a first wireless protocol and the first data of the second digital signal is encoded using a second wireless protocol.	Zheng discloses "wherein the first data of the first digital signal is encoded using a first wireless protocol and the first data of the second digital signal is encoded using a second wireless protocol." See, e.g.:

Claim 21 of the '802 Patent	Prior Art Reference – Zheng

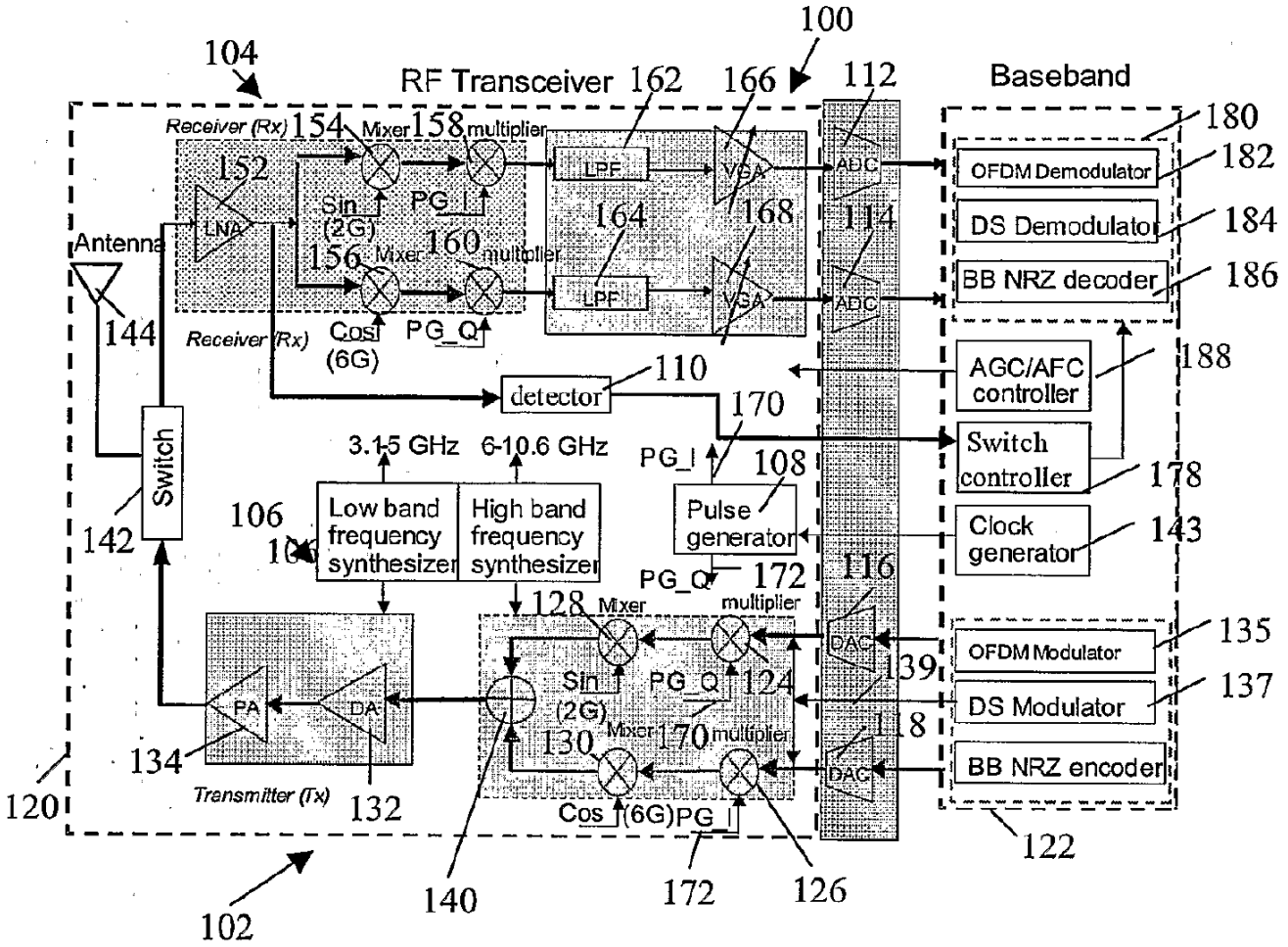


Figure 1

See, e.g., Zheng at Figure 1.

Claim 21 of the '802 Patent	Prior Art Reference – Zheng
	In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027].

Claim 21 of the '802 Patent	Prior Art Reference – Zheng
	The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5)

Claim 21 of the '802 Patent	Prior Art Reference – Zheng
	where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.

Claim 22 of the '802 Patent	Prior Art Reference – Zheng
[22.1] The communication system of claim 17	Zheng discloses all the elements of claim 17 for all the reasons provided above.
[22.2] wherein the second data corresponds to the first data and wherein the power amplifier outputs a third up-converted signal comprising the up-converted first analog signal and the up-converted second analog signal.	Zheng discloses "wherein the second data corresponds to the first data and wherein the power amplifier outputs a third up-converted signal comprising the up-converted first analog signal and the up-converted second analog signal." See, e.g.:

Claim 22 of the '802 Patent	Prior Art Reference – Zheng

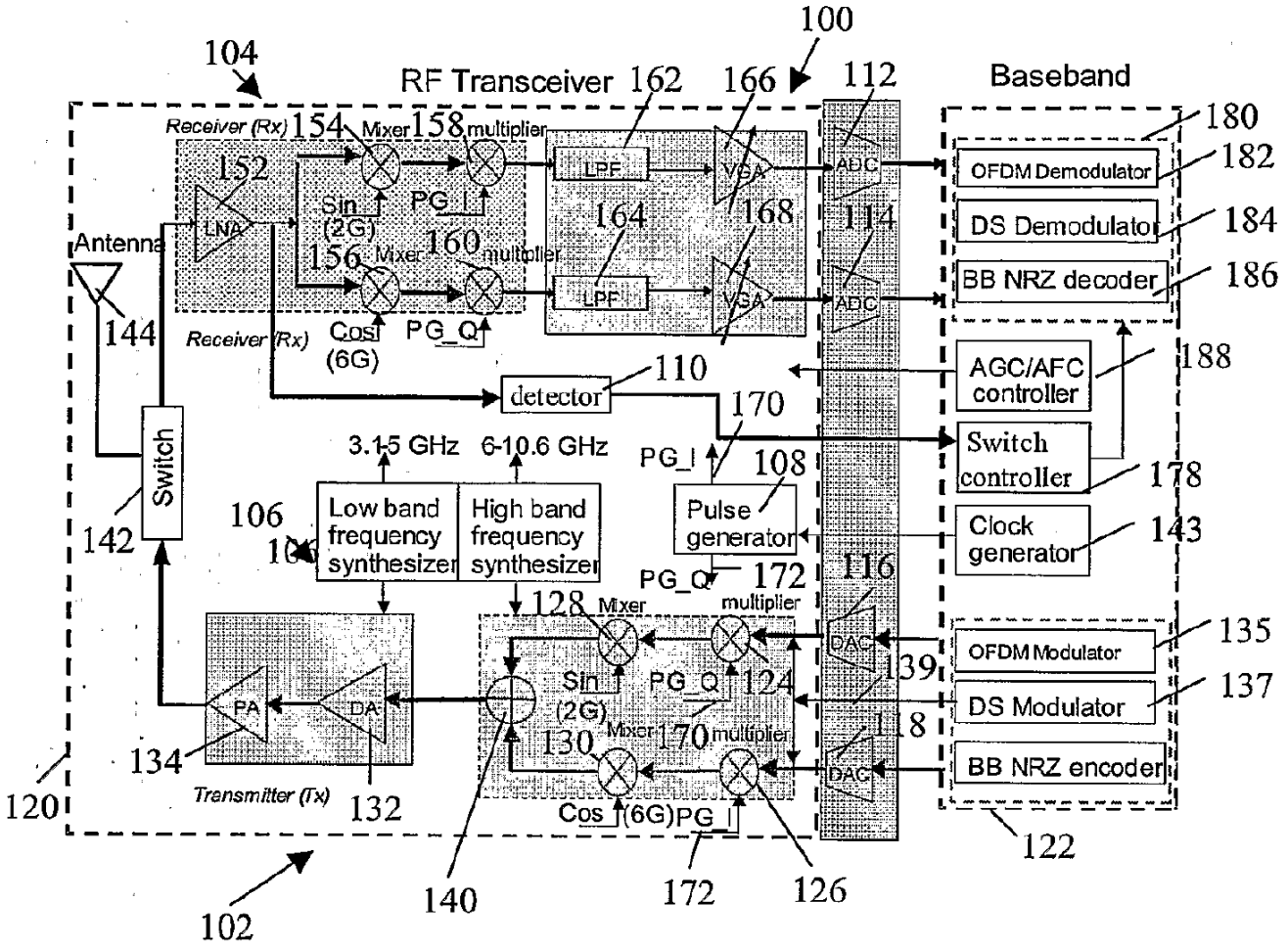


Figure 1

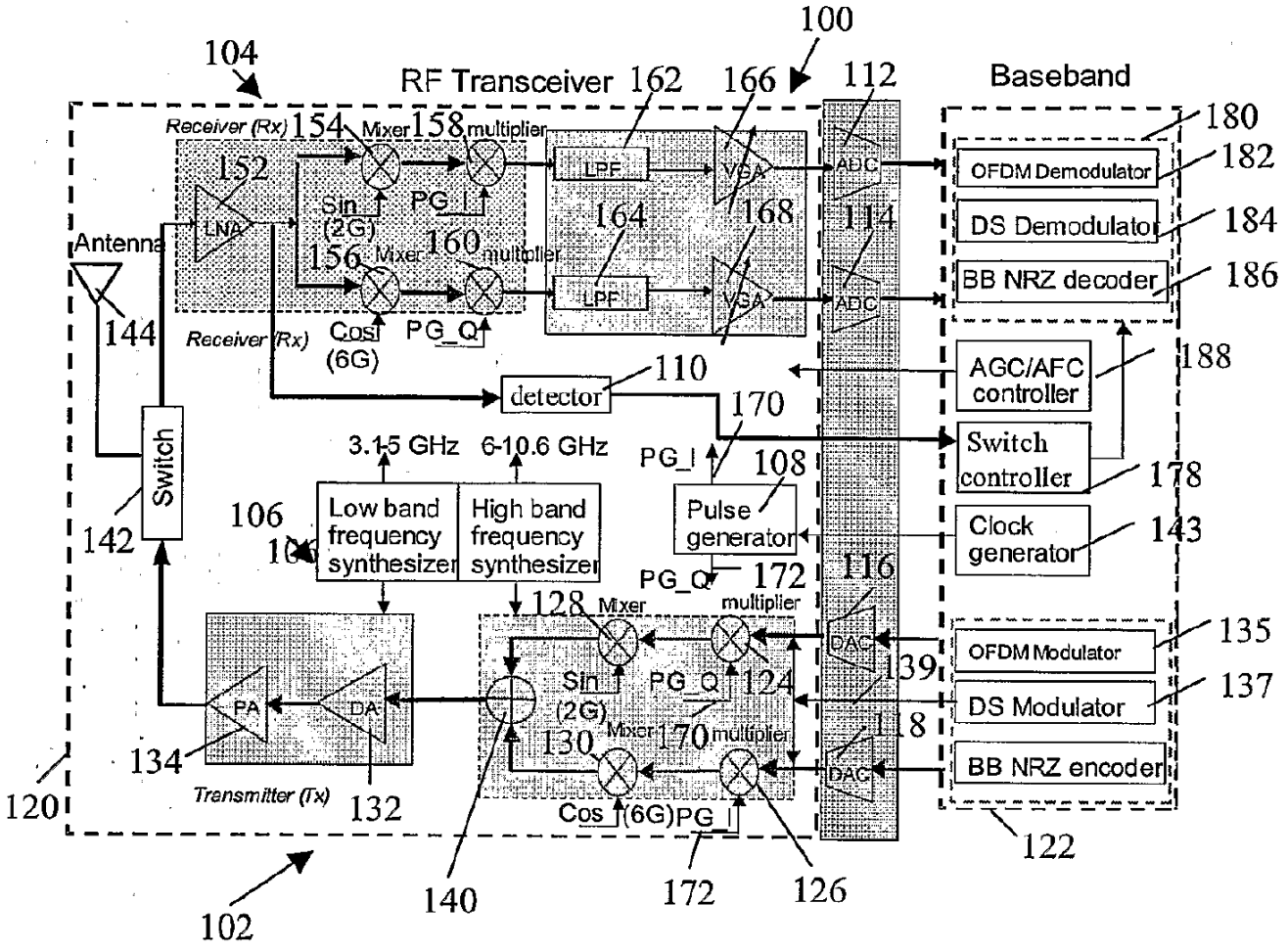
See, e.g., Zheng at Figure 1.

Claim 22 of the '802 Patent	Prior Art Reference – Zheng
	In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027].

Claim 22 of the '802 Patent	Prior Art Reference – Zheng
	The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5)

Claim 22 of the '802 Patent	Prior Art Reference – Zheng
	where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.

Claim 23 of the '802 Patent	Prior Art Reference – Zheng
[23.1] The communication system of claim 17	Zheng discloses all the elements of claim 17 for all the reasons provided above.
[23.2] wherein first and second data to be transmitted comprise a plurality of OFDM symbols, wherein a first symbol is transmitted during a first time slot across the first up-converted frequency range and a second symbol is transmitted during the first time slot across the second up-converted frequency range, and wherein a third symbol is transmitted during a second time slot across the first up-	Zheng discloses "wherein first and second data to be transmitted comprise a plurality of OFDM symbols, wherein a first symbol is transmitted during a first time slot across the first up-converted frequency range and a second symbol is transmitted during the first time slot across the second up-converted frequency range, and wherein a third symbol is transmitted during a second time slot across the first up-converted frequency range and a fourth symbol is transmitted during the second time slot across a second up-converted frequency range." See, e.g.:

Claim 23 of the '802 Patent	Prior Art Reference – Zheng
converted frequency range and a fourth symbol is transmitted during the second time slot across a second up-converted frequency range.	 Figure 1 *See, e.g.*, Zheng at Figure 1.

Claim 23 of the '802 Patent	Prior Art Reference – Zheng
	In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027].

Claim 23 of the '802 Patent	Prior Art Reference – Zheng
	The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5)

Claim 23 of the '802 Patent	Prior Art Reference – Zheng
	where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.

Claim 24 of the '802 Patent	Prior Art Reference – Zheng
[24.1] An electronic circuit comprising:	To the extent the preamble is limiting, Zheng discloses "An electronic circuit comprising." See, e.g.:

Claim 24 of the '802 Patent	Prior Art Reference – Zheng

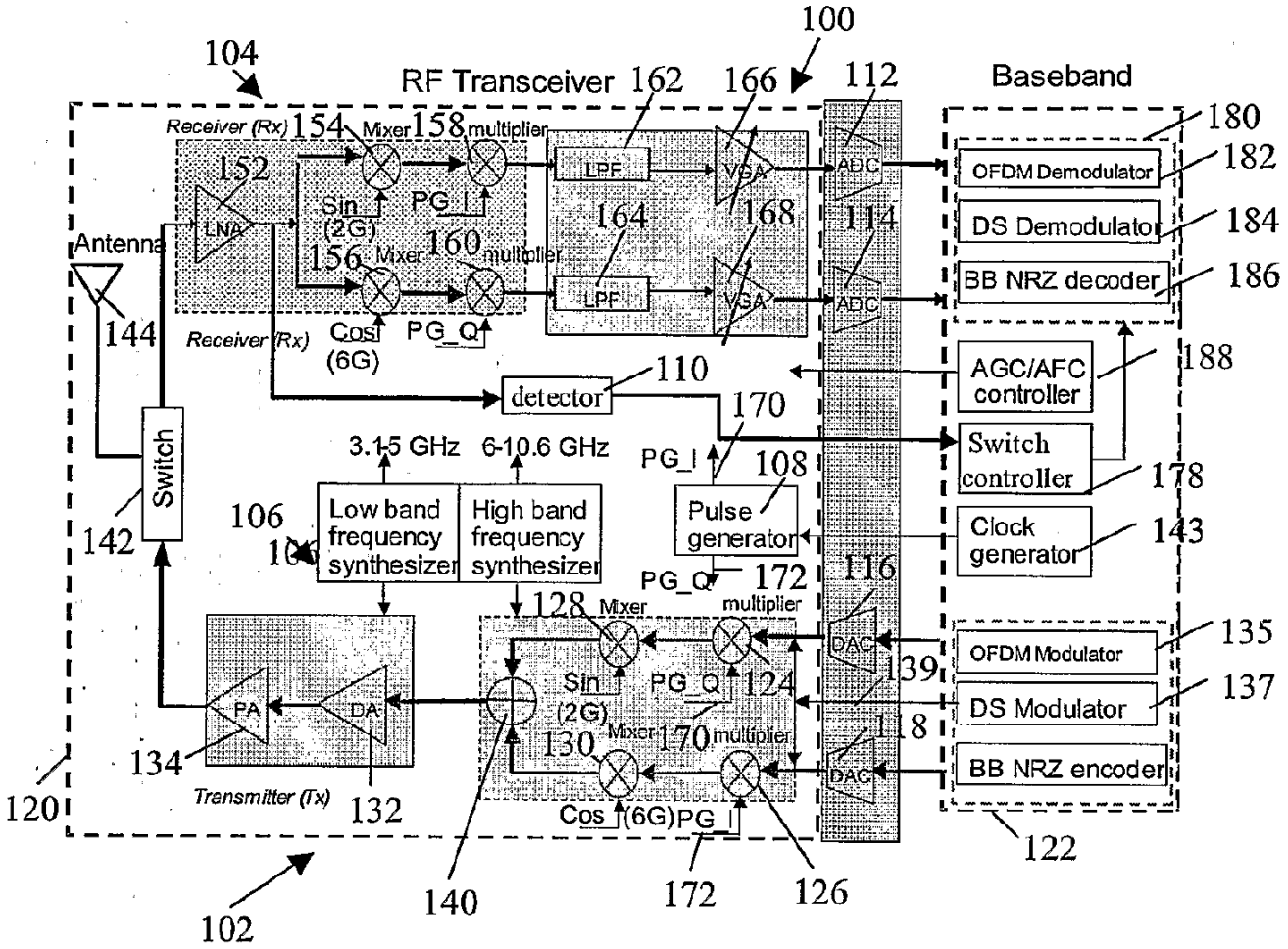


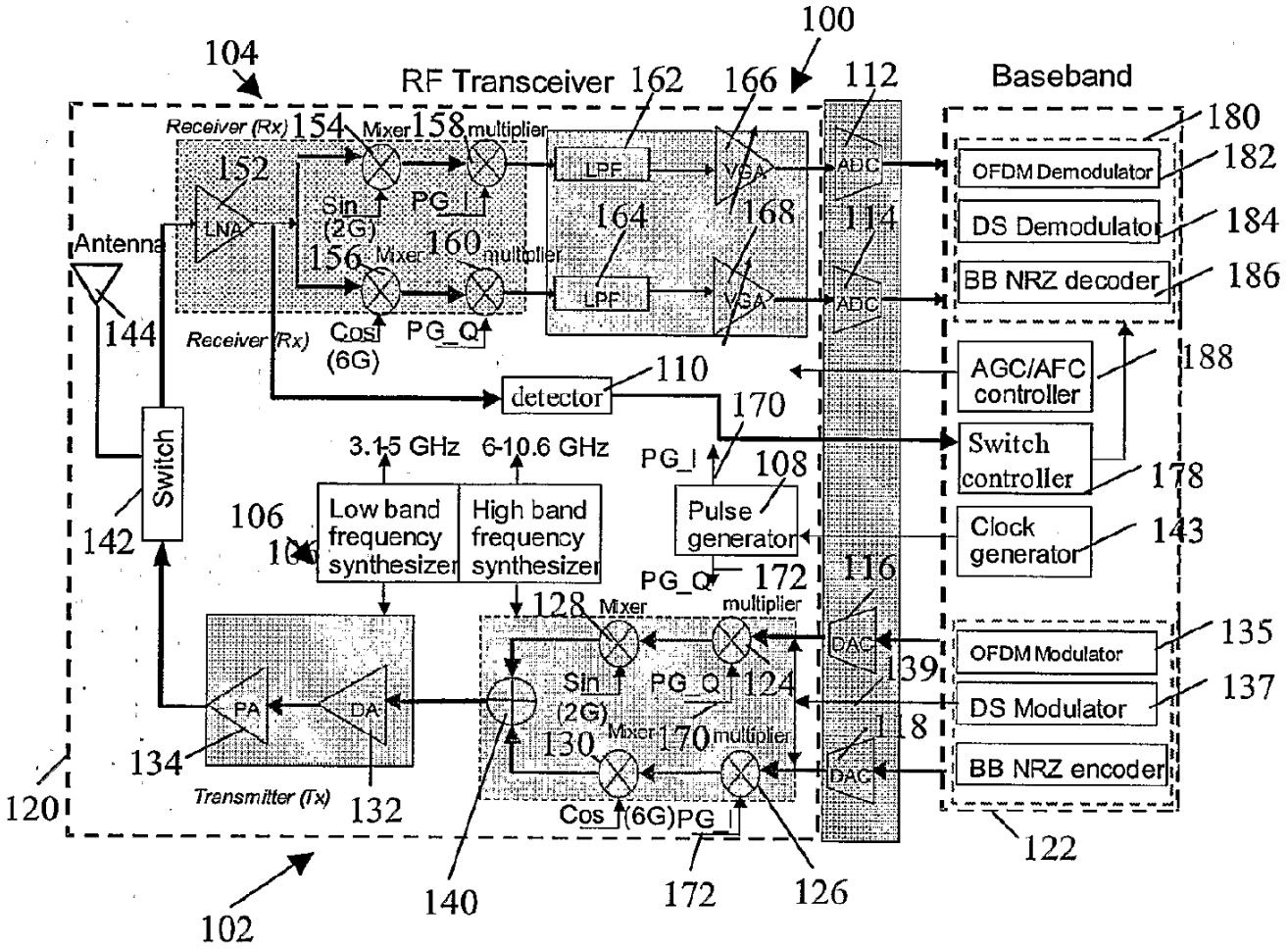
Figure 1

See, e.g., Zheng at Figure 1.

Claim 24 of the '802 Patent	Prior Art Reference – Zheng
	In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027].

Claim 24 of the '802 Patent	Prior Art Reference – Zheng
	The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5)

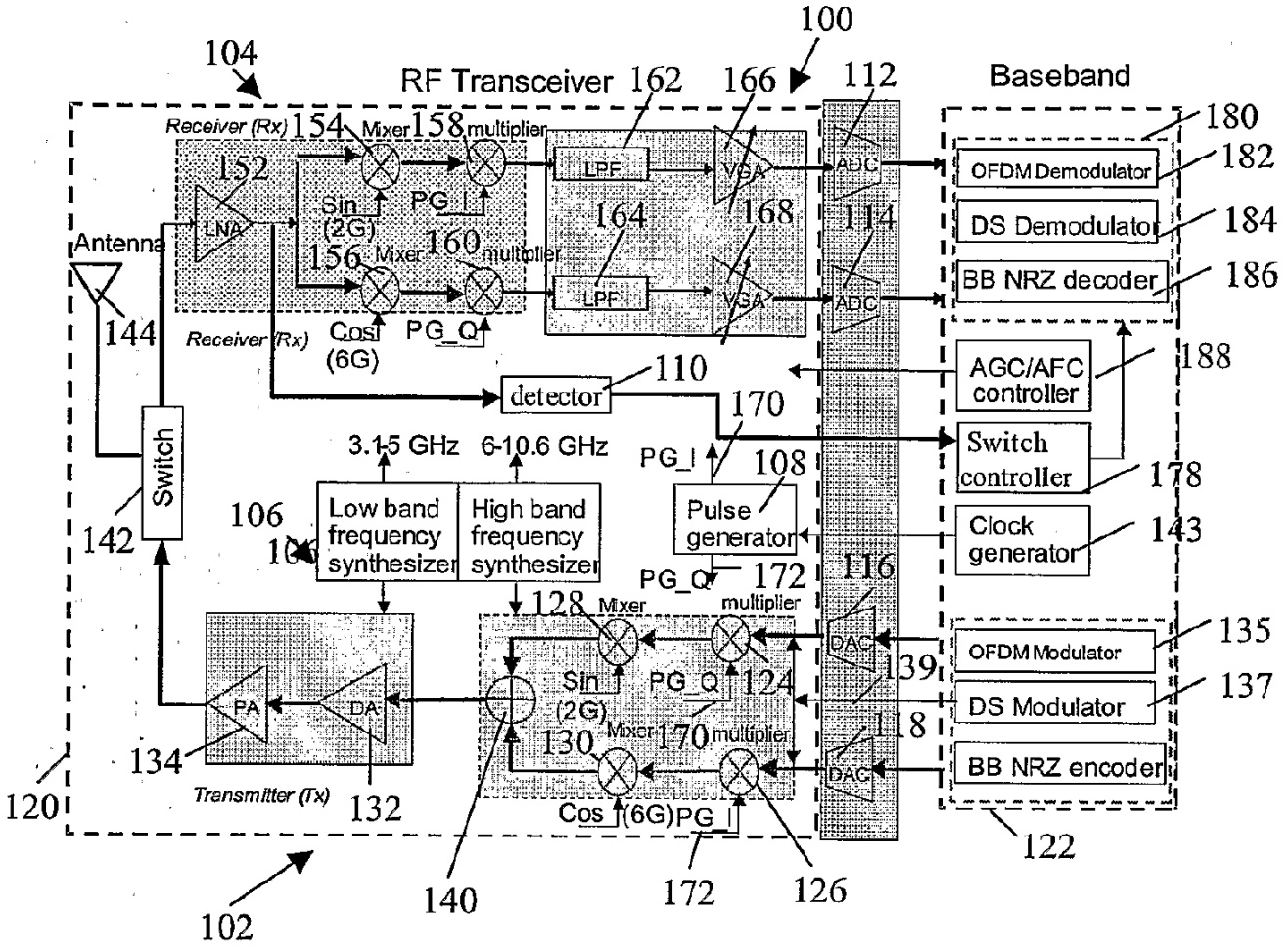
Claim 24 of the '802 Patent	Prior Art Reference – Zheng
	where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.
[24.2] a first down-converter circuit having a first input coupled to receive a first up-converted signal, a second input coupled to receive a first demodulation signal having a first RF frequency, and an output, wherein the first down-converter circuit outputs a first down-converted signal on the first down-converter output;	Zheng discloses "a first down-converter circuit having a first input coupled to receive a first up-converted signal, a second input coupled to receive a first demodulation signal having a first RF frequency, and an output, wherein the first down-converter circuit outputs a first down-converted signal on the first down-converter output." See, e.g.:

Claim 24 of the '802 Patent	Prior Art Reference – Zheng
	 Figure 1 *See, e.g.*, Zheng at Figure 1.

Claim 24 of the '802 Patent	Prior Art Reference – Zheng
	In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See*, *e.g.*, Zheng at ¶ [0024]-[0027].

Claim 24 of the '802 Patent	Prior Art Reference – Zheng
	The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5)

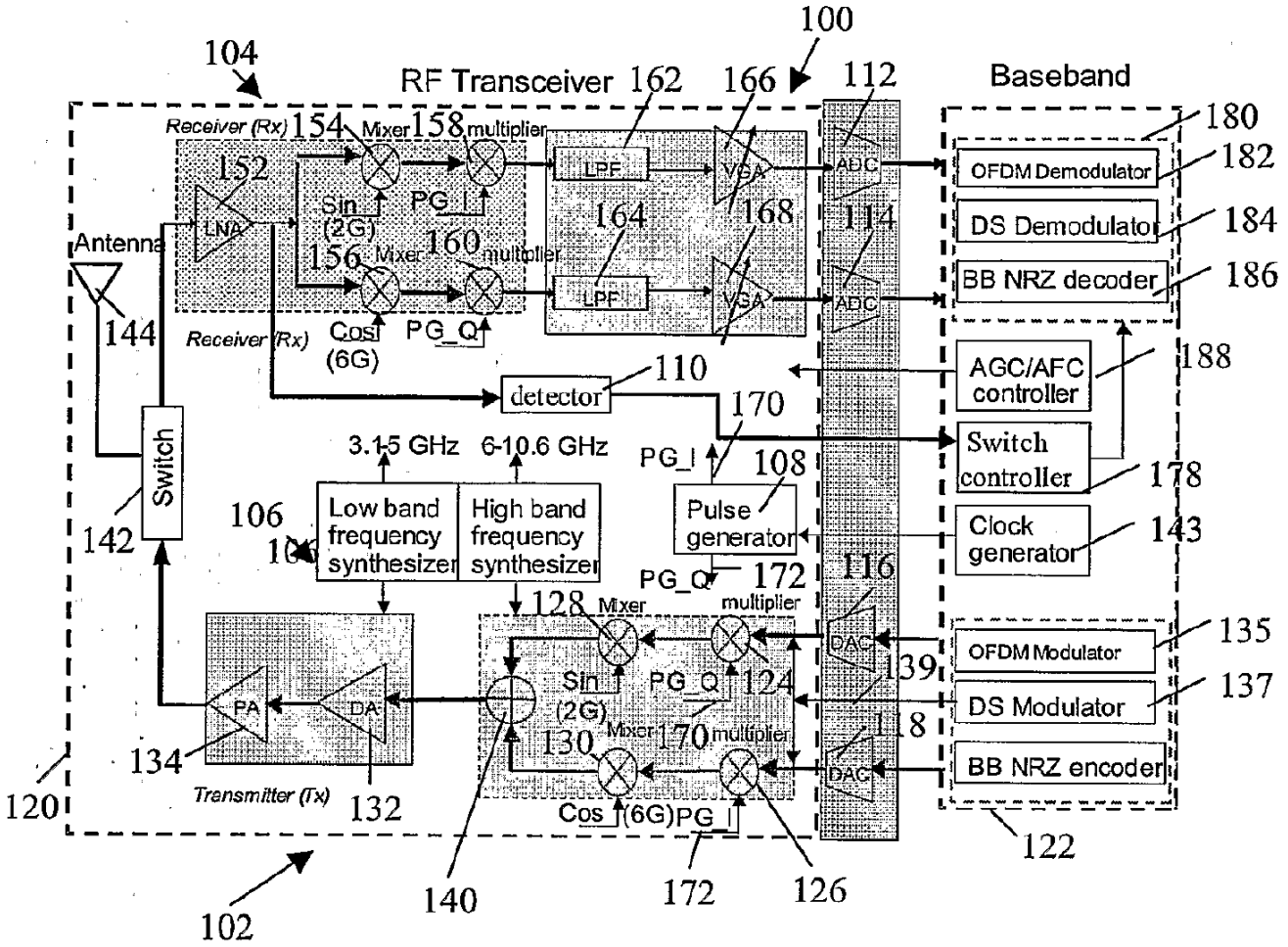
Claim 24 of the '802 Patent	Prior Art Reference – Zheng
	where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.
[24.3] a second down-converter circuit having a first input coupled to receive the first up-converted signal, a second input coupled to receive a second demodulation signal having a second RF frequency different than the first RF frequency, and an output, wherein the second down-converter outputs a second down-converted signal on the second down-converter output, wherein the first up-converted signal comprises a first signal modulated at the first RF frequency and a	Zheng discloses "a second down-converter circuit having a first input coupled to receive the first up-converted signal, a second input coupled to receive a second demodulation signal having a second RF frequency different than the first RF frequency, and an output, wherein the second down-converter outputs a second down-converted signal on the second down-converter output, wherein the first up-converted signal comprises a first signal modulated at the first RF frequency and a second signal modulated at the second RF frequency." See, e.g.:

Claim 24 of the '802 Patent	Prior Art Reference – Zheng
second signal modulated at the second RF frequency; and	 Figure 1 *See, e.g.*, Zheng at Figure 1.

Claim 24 of the '802 Patent	Prior Art Reference – Zheng
	In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027].

Claim 24 of the '802 Patent	Prior Art Reference – Zheng
	The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5)

Claim 24 of the '802 Patent	Prior Art Reference – Zheng
	where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.
[24.4] a filter having an input coupled to the output of the first down-converter and the output of the second down-converter, and in accordance therewith, the filter receives the first and second down-converted signals.	Zheng discloses "a filter having an input coupled to the output of the first down-converter and the output of the second down-converter, and in accordance therewith, the filter receives the first and second down-converted signals." See, e.g.:

Claim 24 of the '802 Patent	Prior Art Reference – Zheng
	 Figure 1 *See, e.g.*, Zheng at Figure 1.

Claim 24 of the '802 Patent	Prior Art Reference – Zheng
	In the described embodiment, a uniform RF transceiver is provided which can be used for design of a radio suitable for MB-OFDM, DS-UWB, and carrier-less impulse radio. Pulse frequency spreading and despreading is adopted to generate the ultra wideband signals and demodulate high rate baseband data. Frequency upconversion and downconversion are utilized to shift the central frequency to the desired subband. The described architecture can adopt the different schemes through switching the corresponding blocks and modulation schemes. The block utility efficiency can be maximized and power consumption can be optimized in the architecture design. As shown in FIG. 1, the proposed RF transceiver 100 includes a transmitter 102, a receiver 104, a frequency synthesizer 106, a pulse generator 108, and a detector 110. Analog to Digital Converters (ADCs) 112, 114 and Digital to Analog Converters (DACs) 116, 118 are used for interfacing the RF transceiver 120 with a baseband processor 122. The transmitter 102 includes two multipliers 124, 126, two mixers 128, 130, one driver amplifier 132, and one power amplifier 134. A series analog baseband data sequence is initially de-multiplexed to parallel data through a serial to parallel SIP conversion in the baseband processor 122. The S/P conversion is implemented in the OFDM Modulator 135 or the DS Modulator 137. The parallel analog data from the DACs 116, 118 can be multiplied with Q and I UWB pulses respectively generated from the pulse generator 108 to form two parallel frequency spreading data sequences, which each occupy at least >500 MHz bandwidth. The two sequences can then be upconverted to different bands by the mixers 128, 130 respectively with a local oscillator (LO) central frequency generated from the multiband frequency synthesizer 106. The frequency upconversion can be an I/Q upconversion or a dual band conversion for MB-OFDM or DS-UWB scheme, respectively. The upconverted signals are combined together at 140 utilising a current or voltage combing circuit 140. A clock generator 143 of the baseband processor 122 is coupled to the I/Q pulse generator 108. *See, e.g.*, Zheng at ¶ [0024]-[0027].

Claim 24 of the '802 Patent	Prior Art Reference – Zheng
	The receiver 104 includes one low noise amplifier (LNA) 152, two mixers 154, 156, two multipliers 158, 160, two low pass filters (LPFs) 162, 164, and two variable gain amplifiers (VGAs) 166, 168. The LNA 152 is used to amplifier the received UWB signals from antenna 144. The mixers 154, 156 can be employed to downconvert the different band signals to the baseband. The signal after LNA 152 is a dualband/multiband signal. Since the input LO signals for the two mixers 154, 156 are different, the mixer 154, 156 output signals can be differentiated. *See, e.g.*, Zheng at ¶ [0029]. The ADC/ DACs 112, 114, 116, 118 can be employed to interface the RF transceiver 120 with the baseband processor 122. Different specifications such as sampling rate, resolution etc. are set for the different schemes. Details of the specifications in the example implementation will be described below. *See, e.g.*, Zheng at ¶ [0035]. In the described example, the generated pulses cover a frequency range (−10 dB bandwidth) from 0.5 to 4 GHz, thus the central frequency is 2.25 GHz. To shift the central frequency to the low frequency band from 3.1 to 4.85 GHz, a 792 MHz LO can be used so that the upconverted frequency is from 1.292 to 4.792 GHz. Through pulse shaping, utilising DA 132, the upconverted frequency can be shaped to the low band from 3.1 to 4.792 GHz (−10 dB band width). Similarly, to shift to the high band from 6.2 to 9.7 GHz, a 6.072 GHz LO can be used so that the upconverted frequency band is from 6.572 to 10.072. The LOs of 792 MHz and 6.072 GHz can be generated form the proposed frequency synthesizer architecture 200 described above with reference to FIG. 2. In the receiver 150, in each band, frequency downconversion is performed first, followed by coherent correlation. This can be expressed as $B \times y(t) \times \cos(\omega_1 t + \varphi_0) \times p_1(t) =^{LPF} x_1(t)$ (4) $B \times y(t) \times \cos(\omega_2 t + \varphi_0) \times p_Q(t) =^{LPF} x_2(t)$ (5)

Claim 24 of the '802 Patent	Prior Art Reference – Zheng
	where B represents the receiver gain. The baseband signals x1(t) and x2(t) are thus recovered, and are converted to a serial sequence x(t) through the parallel to sequential converter implemented in the DS Demodulator 184. *See, e.g.*, Zheng at ¶ [0052]-[0054]. Furthermore, this claim element is obvious in light of Zheng itself, when combined with any of the other references as charted for this claim element in Exs. A-1–A-31, First Supplemental Ex. A-Obviousness Chart, and/or when combined with the knowledge of one of ordinary skill in the art. Motivations to combine may come from the knowledge of the person of ordinary skill themselves, or from the known problems and predictable solutions as embodied in these references. Further motivations to combine references and additional details may be found in the Cover Pleading and First Supplemental Ex. A-Obviousness Chart.